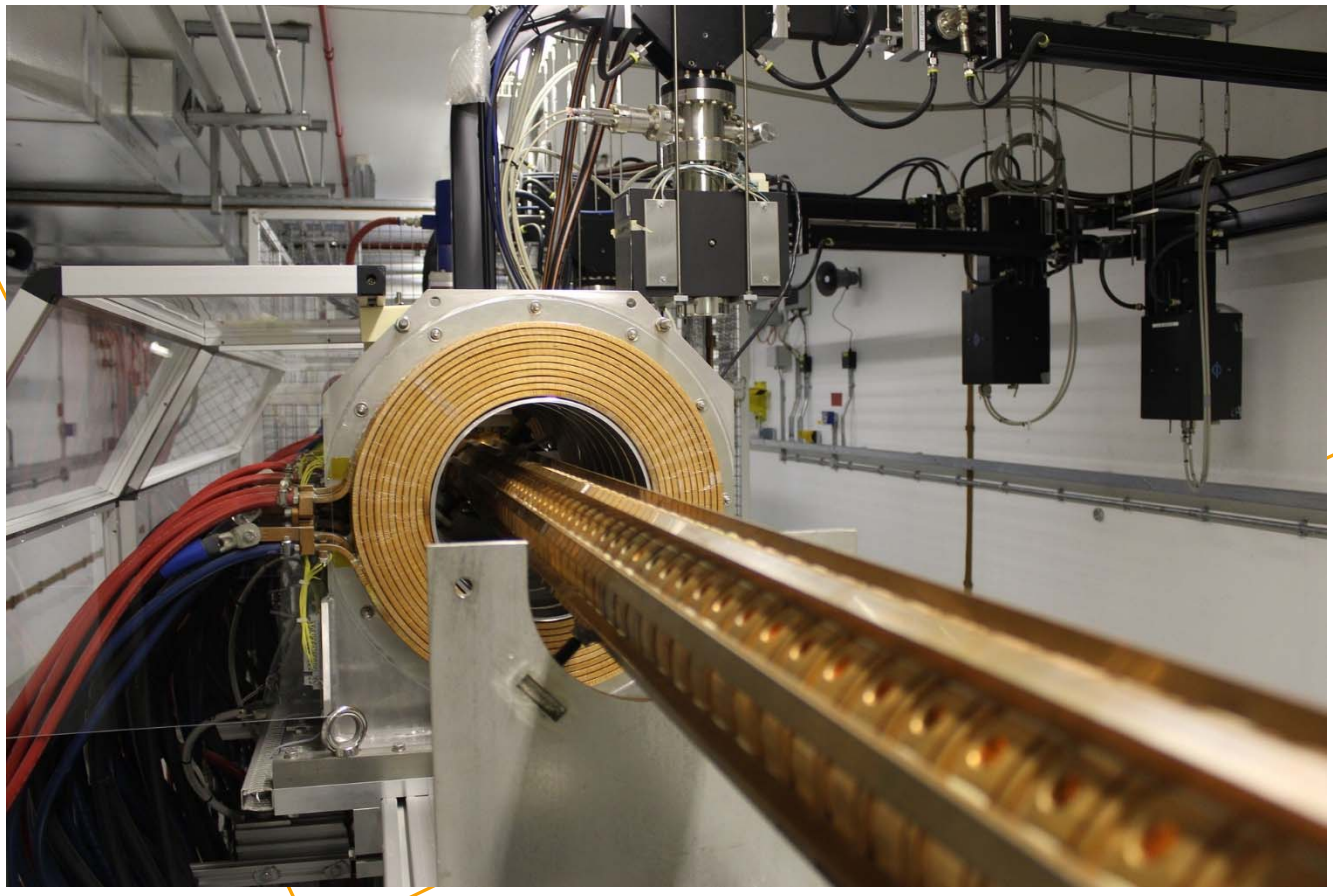

HIGH EFFICIENCY GAN POWER AMPLIFIER DESIGN FOR PARTICLE ACCELERATORS

Echoic Engineering LLC

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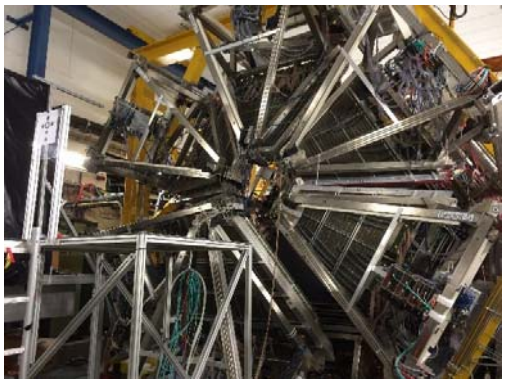
Author: Kelvin Yuk, PhD

CONTACT INFORMATION

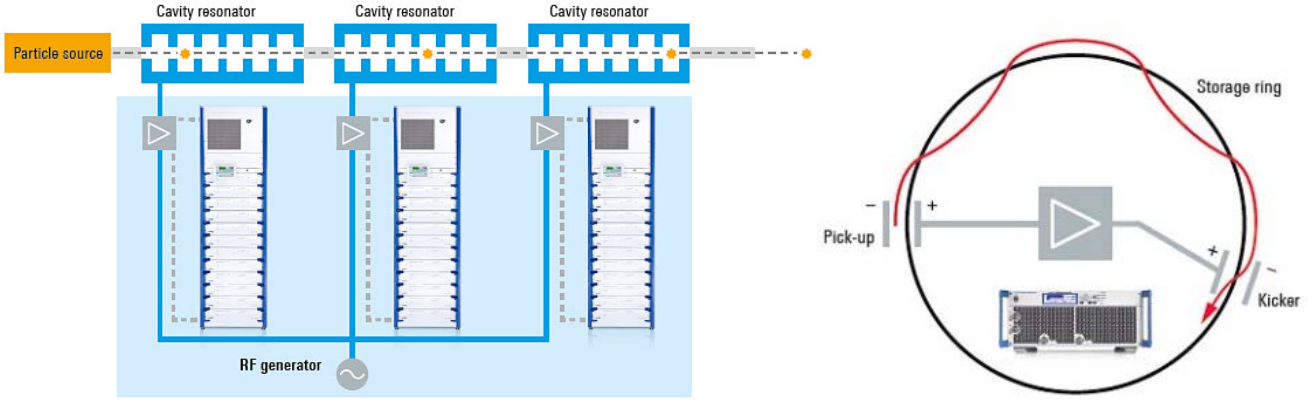
Email: ksyuk@echoicrf.com | **Web:** https://echoicrf.com

TRANSITION TO SOLID-STATE POWER AMPLIFIERS FOR PARTICLE ACCELERATORS

Particle accelerators such as cyclotrons and linear accelerators (LINACs) are widely used as a vehicle for fundamental research in physics as well as energy R&D, medicine, industrial manufacturing and security. A particle beam composed of protons, ions or neutrons can be created by accelerating particles generated from a source using high energy electric fields.



High power kW and MW-class RF power amplifiers (PAs) are used to generate these electric fields in microwave cavity resonators through which the particles pass as shown in Fig. 1a. Furthermore, high power RF amplifiers can refresh the energy of a particle beam by employing a storage ring feedback configuration as shown in Fig. 1b.



(a) (b)

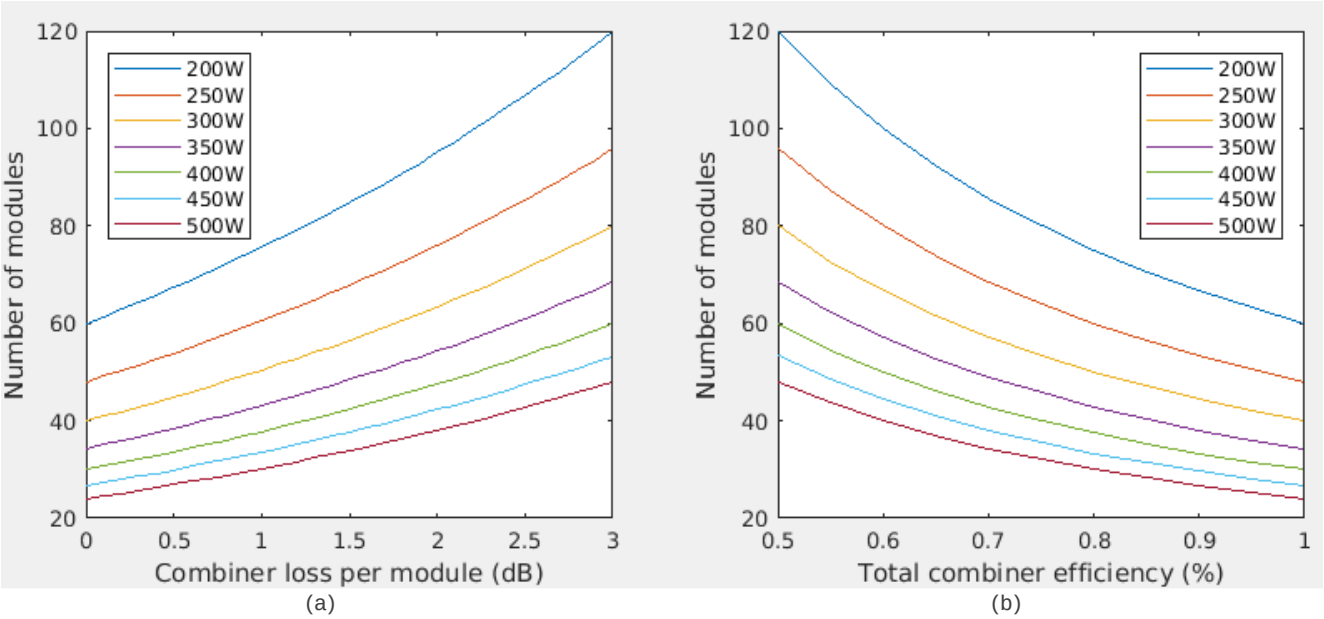
Fig. 1 (a) RF amplifier system used in a particle accelerator chain and (b) RF amplifier used in a feedback loop particle storage ring [1].

Traditionally, particle accelerators found around the world employ the use of tube-based amplifiers including tetrodes, klystrons and traveling wave tubes (TWTs). Tube technology has proven to be robust over many decades and continues to dominate the ultra-high power market. However, they are also large, heavy, cumbersome, expensive to maintain and are potentially dangerous, requiring high-voltage kV power supplies

to operate. Furthermore, considering the aging installations of tube amplifiers, replacement of these with new tubes may not be the most sensible approach for the future evolution of accelerator systems.

With the advent of high power density semiconductors like gallium-nitride (GaN), solid-state power amplifiers (SSPAs) are primed as the future replacements for mature tube amplifiers. GaN HEMT devices are experiencing rapid development in power density, efficiency and longevity and have grown in adoption since its commercial inception around 2008 [2]. Capable of reaching power densities of 12W/mm, GaN devices are seen as the next-generation solid state power technology [3]. Presently, the efficiency of GaN HEMT is similar to that of tube amplifiers, but have the advantages of operating <100V and are relatively inexpensive to replace. Furthermore, GaN technology benefits from the cost savings and size scaling trends of the advancing semiconductor industry. This means that the price per watt will be driven lower as smaller and more efficient devices are introduced.

Despite the recent advances in solid-state technology, limitations on device output power have limited the widespread deployment of kW-class SSPAs [4]-[9]. Such a device will require the collective output of multiple transistors and a complex multi-way combining architecture. This power combining network is challenging to implement as small losses can heavily degrade the output power and efficiency. In order to reach an output of, for example, 12.5kW, one must estimate the number of unit amplifiers needed based on power per unit and combiner loss as shown in Fig. 2. For example, over 70 units are needed if each unit amplifier produces 200W and has an attenuation path of 1dB through the combiner to the output. Interconnecting such a high number of amplifiers is a non-trivial task. Additionally, the power reduction due to self-heating will require a network of cooling hardware, further complicating the system.



(a) (b)

Fig. 2. Number of modules needed to achieve 12kW output versus (a) power combiner losses (dB) and versus (b) power combiner efficiency (%).

Echoic Engineering seeks to develop a state-of-the-art, 12.5kW SSPA achieving > 80% efficiency by designing a high performance unit amplifier and then combining the necessary number of units to achieve a total of 12.5kW. Each unit amplifier will utilize the latest GaN HEMT device and switched-mode transistor operation for high-efficiency. Power combining and high power kW amplifier testing will be performed following the successful validation of a high efficiency unit amplifier. In this white paper, we illustrate the design process for 952.6 MHz, but a similar methodology can be adopted for 563 MHz and 650 MHz.

DESIGNING SOLID-STATE POWER AMPLIFIERS AN ORDER OF MAGNITUDE HIGHER

A Robust Architecture

The overall aim is to develop a microwave power amplifier producing 12.5kW with over 80% efficiency at 952.6 MHz using solid-state devices. As a user-friendly and reliable kW SSPA, the system will have the following design properties [6]:

- A unit amplifier serving as a building block which will employ one or two transistors
- A power combining methodology for transistors with varying degrees of proximity (same board or different parts of rack)
- An effective cooling system for the transistors and combining networks
- An electronic means of activating the amplifier and monitoring the power
- A modular architecture for replacement of damaged transistor units without impairing the others

A conceptualization of the amplifier hardware is illustrated in Fig. 3. The 12.5kW amplifier will serve as the output stage to a RF signal chain and is composed of N unit power amplifier modules, input and output combining networks, a power supply and a control and power monitoring system. Assuming that there are no combiner/divider losses, that the uncompressed gain is ~20dB and that the output power of 12.5kW, or $P_{o,T}$=70.97dBm, occurs at 3dB gain compression, the required drive power is $P_{i,T}$=53.97dBm. This can be provided by a high power pre-amp with uncompressed 20dB gain fed by a medium power driver amp producing P_B=33.97dBm and 20dB gain. This medium power driver will require P_A=13.97dBm from the 952.6MHz RF signal source.

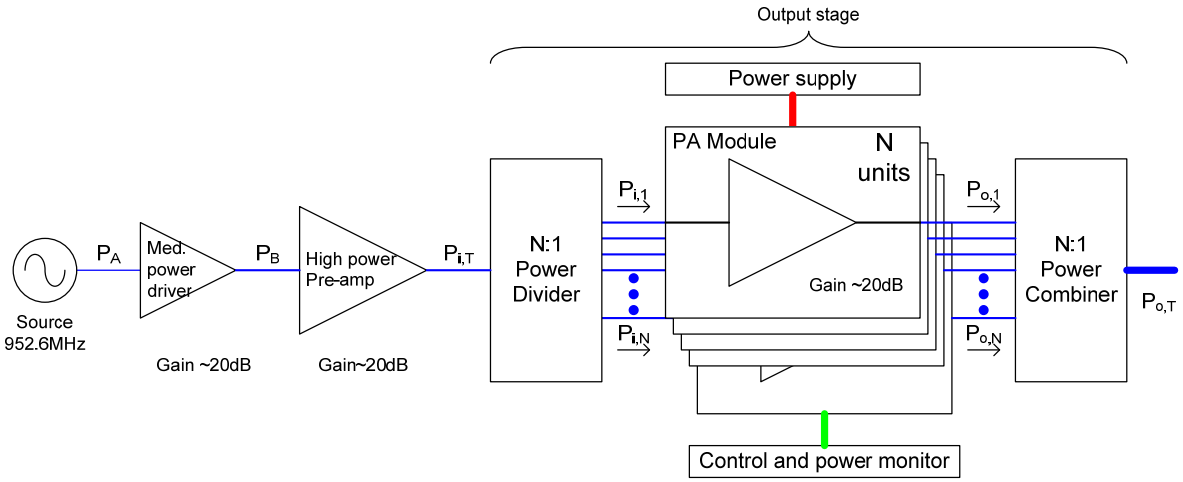


Fig. 3. Block diagram of proposed 12.5kW 952.6MHz power amplifier and driver amplifiers

This white paper describes the design and implementation of the output stage SSPA. The design specifications of the full 12.5kW SSPA are summarized in Table 1. Many design iterations of device characterization, circuit design, tuning and testing will be necessary to achieve the performance required. Echoic Engineering has the experience and technical expertise to achieve these goals.

Table 1. Specifications of the proposed 12.5kW solid-state amplifier

High Power CW Mode (f=952.6 MHz)						
Parameter	**Symbol**	**Test Condition**	**Min.**	**Typ.**	**Max.**	**Units**
System Impedance	Zo		-	50	-	Ohm
Frequency range	f		-	952.6	-	MHz
Input Power	Pi		-	54	57	dBm
Output Power	Po3dB	Output at 3dB gain	70.79	70.97	-	dBm
		compression	12	12.5	-	kW
Gain	Gain		15	20	-	dB
PAE	PAE		80	-	-	%
Harmonics	P2FO		-	-	-30	dBc
	P3FO		-	-	-30	dBc
Dimensions	Height	Full-sized rack	-	78.39	-	inch
	Width	Full-sized rack	-	23.62	-	inch
	Depth	Full-sized rack	-	42.13	-	inch

Currently in Service

A number of recently published solid-state power amplifiers have been successfully deployed at different particle accelerator facilities around the world including the European Spallation Source (ESS) in Sweden [4], the Swiss Light Source (SLS) in Switzerland [5] and BARC-TIFR Pelletron LINAC in India [7]. Characteristics of these kW-class amplifiers with examples up to 150kW CW are summarized in Table 2. We see that most of these use Si LDMOS (laterally-diffused MOSFET) with one using a slightly more exotic VDMOS (vertically diffused MOSFET) and are designed for frequencies up to several hundred MHz. Each amplifier employs the

strategy of designing a power amplifier module producing ~1kW and multiplying these units to achieve the target output. Power amplifier module efficiencies of up to 70% have been demonstrated but have not been reported in every example.

Table 2. Particle accelerator amplifiers using solid-state technology

		Proposed	[4]	[5]	[6]*	[7]	[8]
Frequency		952.6 MHz	352 MHz	500 MHz	72 MHz	325 MHz	83.2 MHz
Pulsed or CW		CW	Pulsed/CW	CW	Pulsed/CW	CW	CW
Pout Total		12.5 kW	10 kW	65 kW	150 kW	8 kW	3.2 kW
PA module	Technology	GaN HEMT	Si LDMOS	Si LDMOS	Si VDMOS	Si LDMOS	Si LDMOS
	# of transistor packages	2	1	1	4	1	1
	Pout	1 kW	1 kW	750 W	1.45 kW	1 kW	1.6 kW
	Efficiency	80	61	63	-	70	-
	Substrate	Rogers 6035HTC	Rogers 3003	-	-	eps=3.5	-
Output combiner	Type	Gysel	Gysel	-	-	Wilkinson	Wilkinson
	Realization	Planar	Planar	Radial	Radial	Radial	Planar
	Medium	Rogers 6035HTC	TMM3	-	Coaxial	Coaxial	Teflon
*several designs, reporting the one with most details							

Comparatively speaking, 952.6 MHz for the amplifier proposed here is on the upper spectrum. Although kW-class GaN amplifiers have not yet been deployed for particle accelerators, they exist for other applications like radar [10] [11] and there is strong evidence that they can be applied here. Furthermore, new devices from GaN foundries are being released which can produce as much as 1500W [12]. Therefore, our goal of >80% efficiency is relatively ambitious.

From these works, there seems to be no dominant means of power combining multiple unit amplifiers although low-loss radial, coaxial combiners are preferred for their low-loss characteristics. Furthermore, some indication of the circuit substrate to be used for the amplifier and power combiner can be gained from these references.

Designing for the Future

Interest in migrating tube-based kW amplifiers to solid-state is stronger than ever. However, there is still a significant gap in knowledge before full adoption can take place.

Reports on the high power density (W/mm) of GaN devices are often accompanied by data from small periphery transistors [3]. However, a wide periphery device is needed to produce usable power in the range of several hundreds of watts. The RF power density is inversely related to the device periphery due to stronger self-heating, which degrades transconductance, and to larger parasitics which attenuates the usable gain. Furthermore, many GaN devices on the market are advertised as pulsed devices [13], [14] and do not make claims about CW operation. It is important to gain an understanding of GaN for CW operation as it will indicate the usable power and long-term reliability for many commercial systems [15].

Most commercially available high power GaN HEMTs producing >100W are designed for class AB, which provides a good balanced of linearity and efficiency for cellular base-station and broadcast applications. However, linearity is not as critical as efficiency and power in particle accelerator amplifiers and therefore a high efficiency switched-mode is preferred. Although many high efficiency GaN PAs have been published for

wireless applications [16]-[18], only a few have demonstrated switched-mode operation with output >100W [19]. The is due to self-heating which degrades the gain/efficiency and device parasitics that limit how fast the transistor can turn on and off. Techniques to adapt these high power devices for switched-mode Class D, E, F and inverse-F (F^{-1}) will be employed by using load tuning and harmonic manipulation [20]. We use the vendor's nonlinear model to the transistor's efficacy in switched-mode operation. If the necessary waveform class can be achieved in simulation, it might be achievable on the actual device. Furthermore, any internal matching done on the devices will be compensated using the appropriate matching networks.

Insertion loss of even fractional dB due to electrical resistivity, path mismatch and thermal degradation not only reduces the combiner efficiency but also bottlenecks the overall amplifier's performance. According to Fig. 3, the total output power is

$$P_{o,T} = \sum_{k=1}^{N} \eta_{combiner,k} P_{o,k}$$

$$\text{and } \eta_T = P_{o,T}/P_{DC}$$

where $\eta_{combiner,k}$ is the output combiner efficiency of the kth PA module and η_T is the total output amplifier drain efficiency. Furthermore, the total input power is

$$P_{i,T} = \sum_{k=1}^{N} \eta_{divider,k} P_{i,k}$$

where $\eta_{divider,k}$ is the input divider efficiency and the total power added efficiency is given by

$$PAE_T = \left(P_{o,T} - P_{i,T}\right)/P_{DC}.$$

Therefore, the PAE is heavily dependent on finding a low loss, high isolation method of N-way power combining. This will include an investigation of circuit topologies, processing techniques and materials with superior heat transfer and high thermal conductivity.

Finally, a knowledge gap exists in the best method of thermal reduction for such a large number of high power devices. Water-cooled, air-cooled or a combination of techniques may be the answer.

The Urgent Need and Beyond

There are over 30,000 particle accelerators in existence [21] and some of the most well know accelerators like CERN are responsible for major discoveries in science [22]. However many of these are based on tube amplifiers and are very old. Failure to properly maintain and upgrade these particle accelerators with modern electronics will result in extended downtime, the loss of productivity and the loss of government funding for those projects. Efforts to reduce the size of particle accelerators may be enabled by reduced size SSPA technology in the future [23].

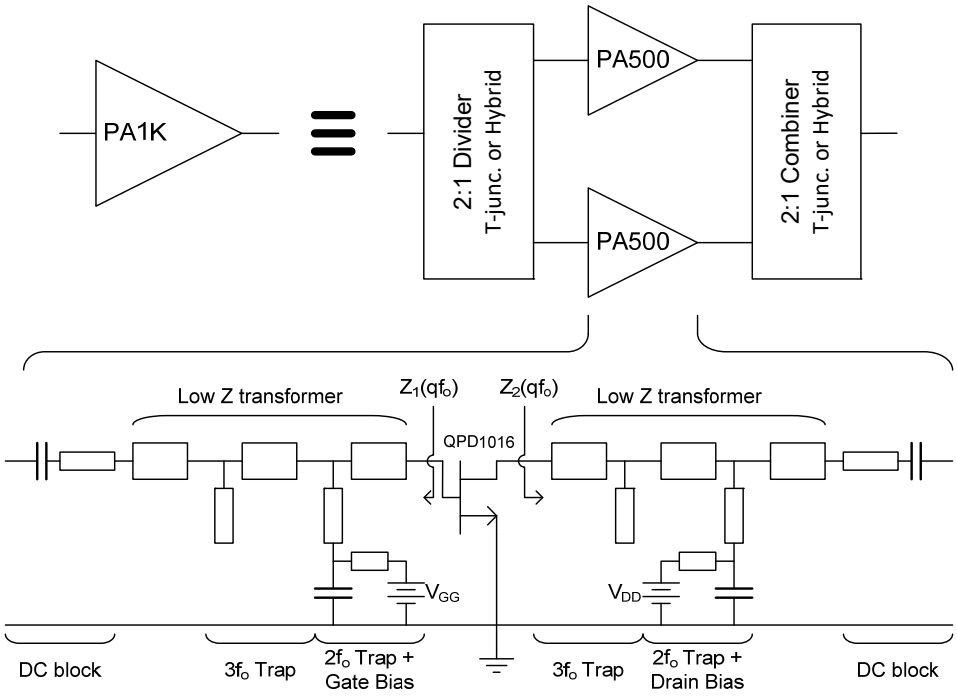
The continued use of tube-based amplifiers may be an acceptable medium-term solution [24], but is non-optimal for the long term. Continued reliance on tubes would stifle the growth of solid-state in this important use-case as GaN continues to chop away at the high power RF market. It is imperative that we develop the appropriate techniques and workflows for implementing kW/MW SSPAs to prepare for the eventual supplanting of tubes by GaN.

Beyond particle accelerators, modern, high power amplifier solutions are needed in a wide variety of applications in multiple industries. In the commercial wireless industry, high power PAs are used in satellite communications, broadcast television and cellular base-stations. In the medical arena, high power PAs may be found in MRI, spectrometry, hyperthermia treatment and microwave ablation. Finally, in the aerospace/defense industry, high power PAs are needed for land-mobile radio; radar, where the range is dictated by the power of the interrogating signal; and electronic warfare (EW) applications like signal jamming, which require compact, vehicle-mountable solutions. The elegance of the modular design means that techniques developed for the unit amplifiers can easily be manifested for any of these other applications depending on the power and frequency requirements. Block diagrams for GaN in some of these RF systems are provided in [25].

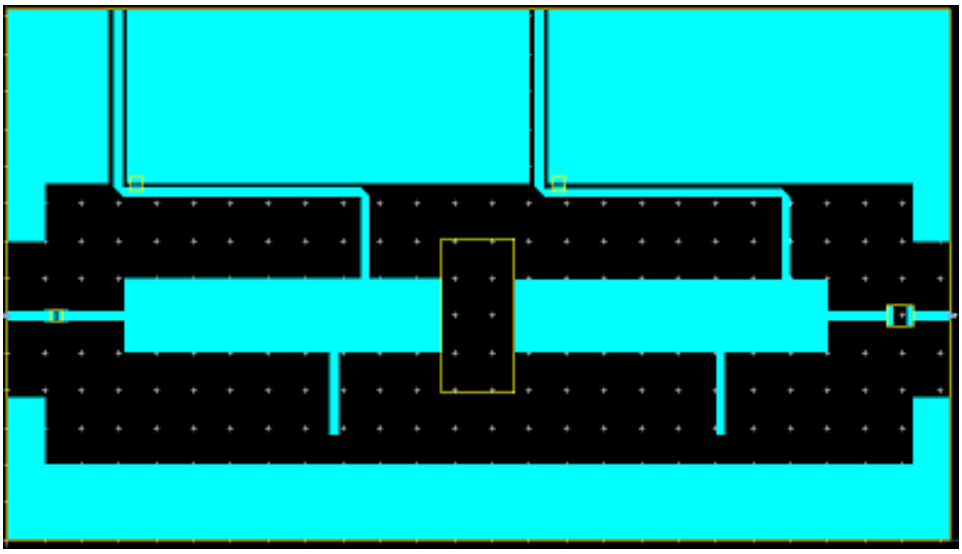
ROBUST DESIGN OF THE SSPA

A Hierarchical Rationale

The 12.5kW PA has a number of critical components and subsystems. These subsystems include the unit power amplifier module, the output power combiner, the biasing and power monitoring system and the cooling system. At the heart of the PA system is the unit amplifier. We propose a unit high power amplifier capable of producing 1kW (PA1K) as a sub block for the 12.5kW system as shown in Fig. 4a. The core amplifier contains two 500W amplifiers (PA500) and integrated planar power combining networks on a single baseplate. In the following section, we will describe the detailed design of the PA500 500W single transistor amplifier to be used inside of the 1kW PA module. We will then multiply the number of these amplifiers and power combine them to demonstrate the feasibility and constraints of the 12.5kW SSPA.



(a)



(b)

Fig. 4. Unit power amplifier topology for the 12.5kW amplifier (a) representation of the PA block, the divider and combining structure and the circuit schematic for a single-transistor package amplifier (b) layout of the microstrip amplifier.

Transistor Selection and Procurement

The initial step is to find an appropriate transistor capable of producing several hundreds of watts to perform a detailed class-F amplifier study. A survey of available transistors operating at 952.6MHz was conducted across semiconductor manufacturers. The two main technologies are Si LDMOS and GaN HEMT, which can be housed in a single package (one transistor) or a "gemini" package (two transistors in the same package). The package type is important as it indicates a possible use case as a push-pull amplifier. The results of this survey are shown in Table 3. We would like to focus on the GaN HEMTs in this initial study although Si LDMOS can be revisited in the event that GaN HEMTs are not reliable enough. GaN HEMTs have power densities as high as 12W/mm and are seen as the future of high power solid-state RF circuits [3] but may not yet be mature enough for long term use.

Table 3. Commercially-available solid-state devices producing > 200W at or around 952.6MHz

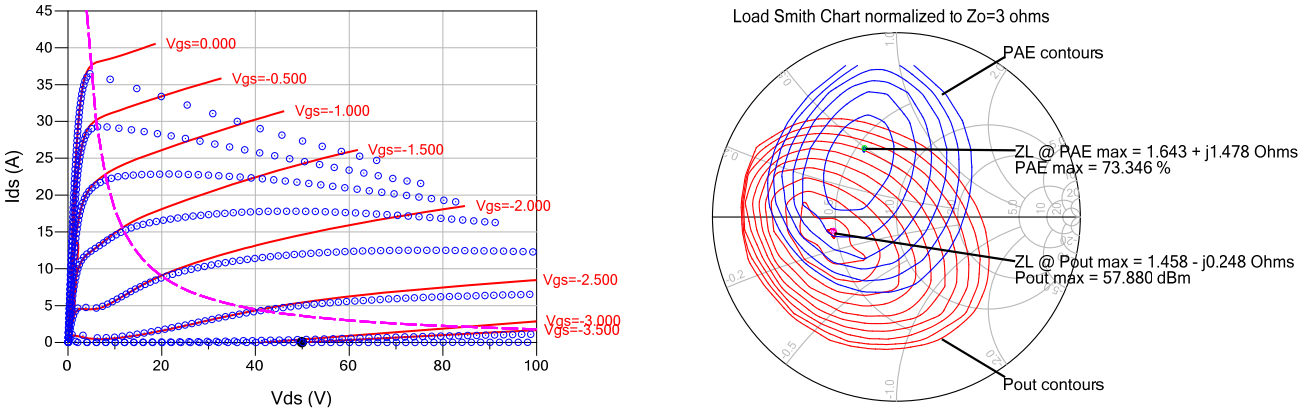
Manufacturer	Part	Freq (GHz)	Pout (W)	Technology	Package
Ampleon	BLF10H6600PS	0.4 - 1	250	Si LDMOS	Dual
Ampleon	BLF647P	1.3	200	Si LDMOS	Dual
MACOM	NPT2024	DC - 2.7	200	GaN HEMT	Dual
MACOM	MAGx-101214-500L00	1.2 - 1.4	500	GaN HEMT	Single
MACOM	MAGx-100027-300	0.001 - 2.7	300	GaN HEMT	Dual
NXP	MHT1002N	0.915	350	Si LDMOS	Dual
Qorvo	QPD1016	DC - 1.7	680	GaN HEMT	Single
Qorvo	QPD1025	1.0 - 1.1	1500	GaN HEMT	Dual
Wolfspeed	CGHV14250F	0.5 - 1.6	250	GaN HEMT	Single
Wolfspeed	CGHV14500F	0.5 - 1.8	500	GaN HEMT	Single
Wolfspeed	CGHV14800F	1.2 - 1.4	800	GaN HEMT	Single
Wolfspeed	CGHV40200PP	DC - 2	250	GaN HEMT	Dual

Development of High Efficiency Class-F or Inverse Class-F PA

The Qorvo QPD1016 has been selected for the analysis and design of a single-transistor class-F amplifier [26]. The transistor model is developed by Modelithics and the design is performed in Keysight ADS 2015. Assuming that the model is accurate, successful design of this amplifier will establish several things: (1) that the selected transistor can provide the necessary power and (2) that class-F operation and high efficiency > 80% can be achieved.

Transistor Characteristics and Evaluation

The pulsed and static IV characteristics of the device model will provide insight on the power capabilities of the device and also illustrate the detrimental effects of self-heating. GaN devices suffer from an extreme case of self-heating due to the high power density of the device (high dissipated power within a small physical region), making them difficult to cool down. This can be observed by comparing the static IV characteristics (blue) and pulsed IV characteristics (red) shown in Fig. 5a.



(a) (b)

Fig. 5. (a) Pulsed (red) and static (blue) IV characteristics of QPD1016 and 180W constant power contour (magenta) and (b) Load-pull contours for Pout (red) and PAE (blue)

The pulsed IV should be used for PA design and resemble "normal" transistor IV characteristics, while the static IV demonstrate varying degrees of self-heating since each data point has a different dissipated power, Pdiss=Ids*Vds. Dr. Yuk is a pioneer in the use and understanding of PIV for GaN device modeling [27]. The important takeaway is that the IV curves deviate at a constant dissipated power contour of ~180W (Fig. 5a magenta). This self-heating can result in performance degradations at RF if not properly accounted for in the design. We also provide a first-pass load-pull simulation of the device to find the maximum Pout=57.88dBm (613W) and PAE=73.35% in class-B bias as shown in Fig. 5b. A PAE=73.35% at Class-B implies that the device can possibly reach >80% for the class-F design.

Analysis for Switched-Mode Class-F Operation

The QPD1016 model was analyzed using harmonic load- and source-pull simulations (Fig. 6a) that allow for the independent manipulation of the harmonic terminations until a specific outcome is achieved. In our case we determine the optimal harmonic load impedances $Z_2(qfo)$, where q is a harmonic of interest, until high efficiency class-F waveforms are observed at the intrinsic drain.

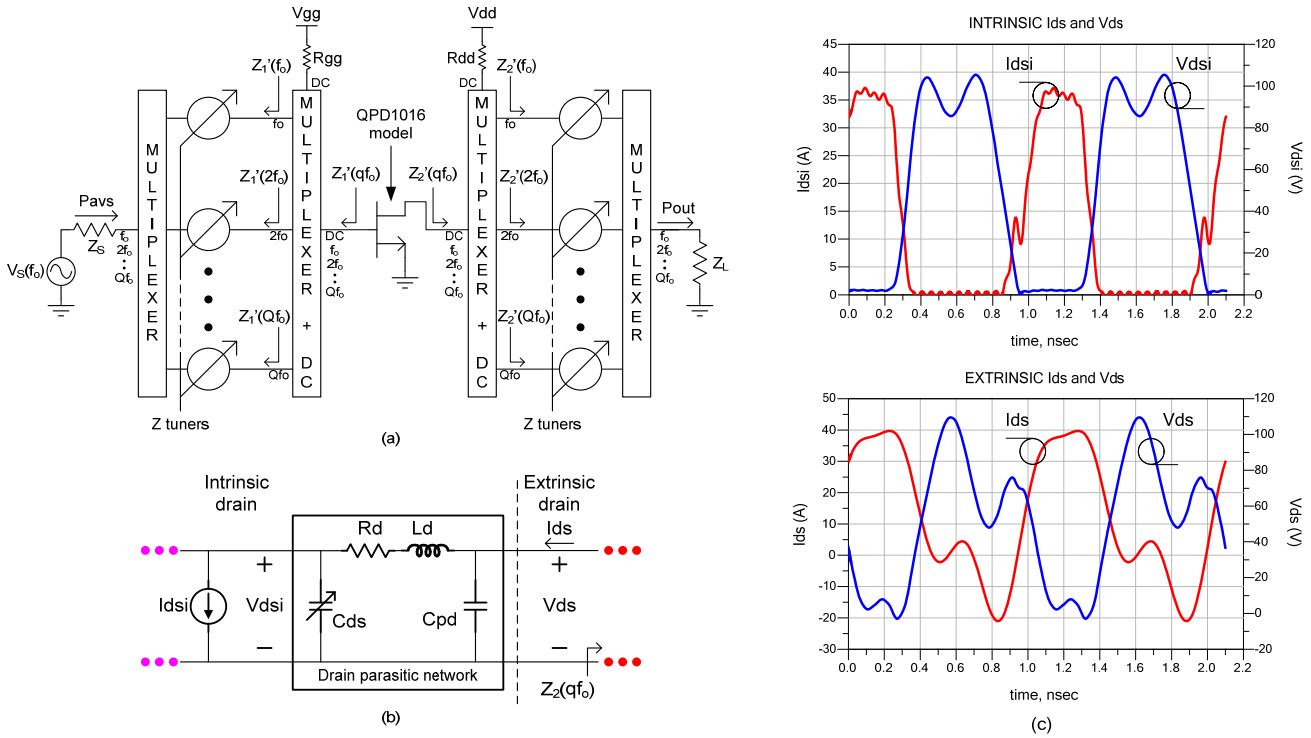


Fig. 6. (a) Harmonic load- and source-pull analysis to achieve Class-F operation on GaN HEMT device (b) intrinsic and extrinsic drain locations for class-F observation and (c) Class-F waveforms achieved on the QPD1016 intrinsic (top) and extrinsic (bottom) drain current and voltage

The intrinsic drain current (Idsi) and voltage (Vdsi) exist at an imaginary terminal inside the model, while the extrinsic drain current (Ids) and voltage (Vds) are physically accessible at the package terminal (Fig. 6b). The intrinsic and extrinsic drains are separated by an internal network of elements consisting of package parasitics (Rd, Ld, Cpd) and the nonlinear drain-source capacitance (Cds) shown in Fig. 6b. For class-F operation, the Idsi resembles a half-rectified sine wave while Vdsi resembles a square wave as shown in Fig. 6c (top). This is further verified by the harmonic content of Idsi which has high 2fo (-7.495dBc) and low 3fo (-23.463dBc) and by the harmonic content of Vdsi which has low 2fo (-26.931dBc) and high 3fo (-10.444dBc). These class-F waveforms are distorted by the parasitic network and therefore cannot be observed at the extrinsic drain as shown in Fig. 6c (bottom). Under this class-F operation we obtain a PAE=85.46% at Pout=57.19dBm (523.6W).

Class-F amplifier using QPD1016

The harmonic load, Z_2(qfo), and source, Z_1(qfo), impedances were synthesized into low-loss microstrip networks using the substrate model for Rogers 6035HTC substrate (20mil thickness, 2oz. copper, eps=3.6) and optimized for performance. The circuit schematic and layout are shown in Figs. 4a and 4b, respectively. A size reduction can be performed later by introducing lumped elements to take the place of distributed elements in the matching networks.

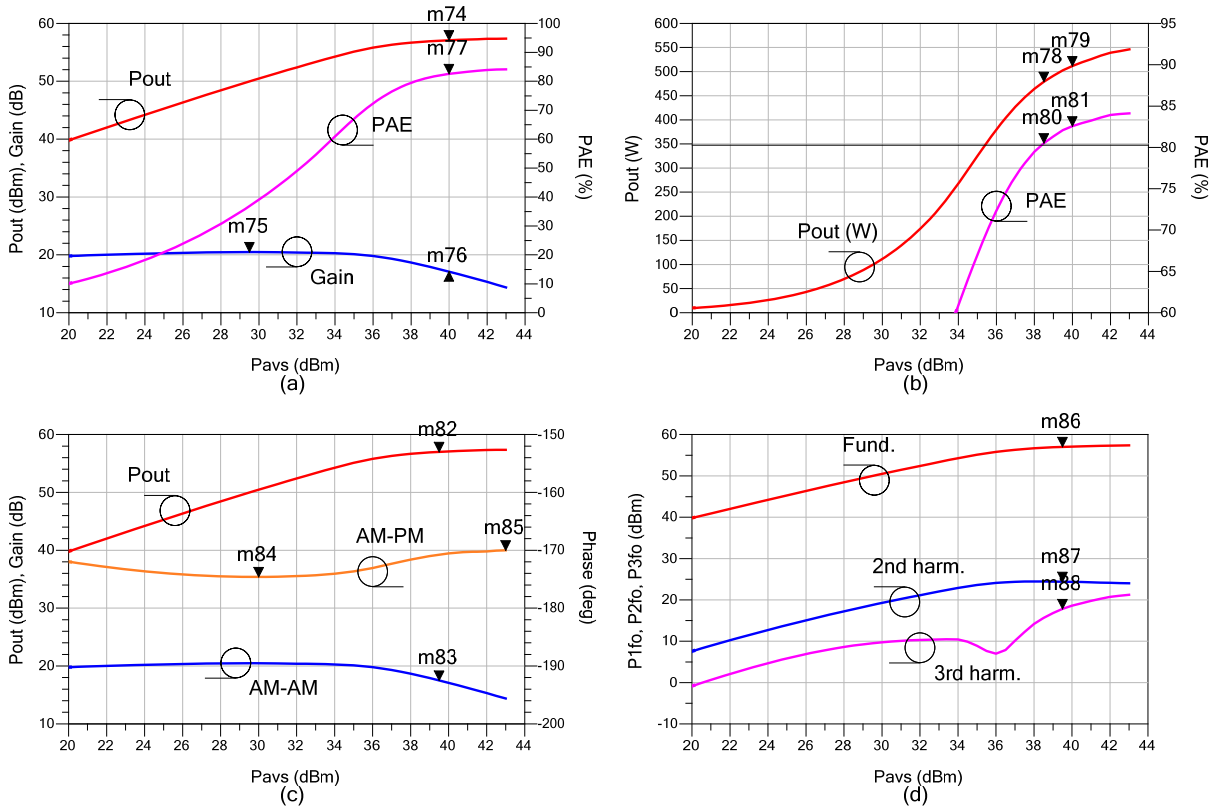


Fig. 7. Performance of the QPD1016 amplifier using Rogers 6035HTC 20mil (a) Pout (dBm), Gain (dB) and PAE (%) (b) Pout in watts (c) AM-AM and AM-PM curves (d) first, second and third harmonic output.

The simulated performance of the microstrip-based amplifier is shown in Fig. 7. As seen in Fig. 7a, the peak gain is 20.47dBm and Pout=57.089dBm (511W) at a 3dB gain compression of Pavs=20dBm. This gives a corresponding PAE=82.568%. The PA has PAE > 80% for Pout > 478W as shown in Fig. 7b. Furthermore, the linearity of the amplifier is indicated by the AM-AM and AM-PM plots on Fig. 7c. It has < 5 degree phase deviation up to Pavs=43dBm and has < 1dB gain variation up to Pin=38dBm. Hence this ~500W class-F PA is very linear.

Power Combining

The power combing approach and implementation is vital to the overall 12.5kW PA performance. The key performance parameters include (1) low insertion loss (IL) and low return loss (RL) to prevent degradation of the Pout and PAE (2) balanced performance between multiple input/outputs and (3) good isolation such that the failure or removal of one unit amplifier does not impact the others. Two popular power combining schemes are multi-level 2-way combiners (corporate) as shown in Fig. 8a and a single N-way combiner as shown in Fig. 8b.

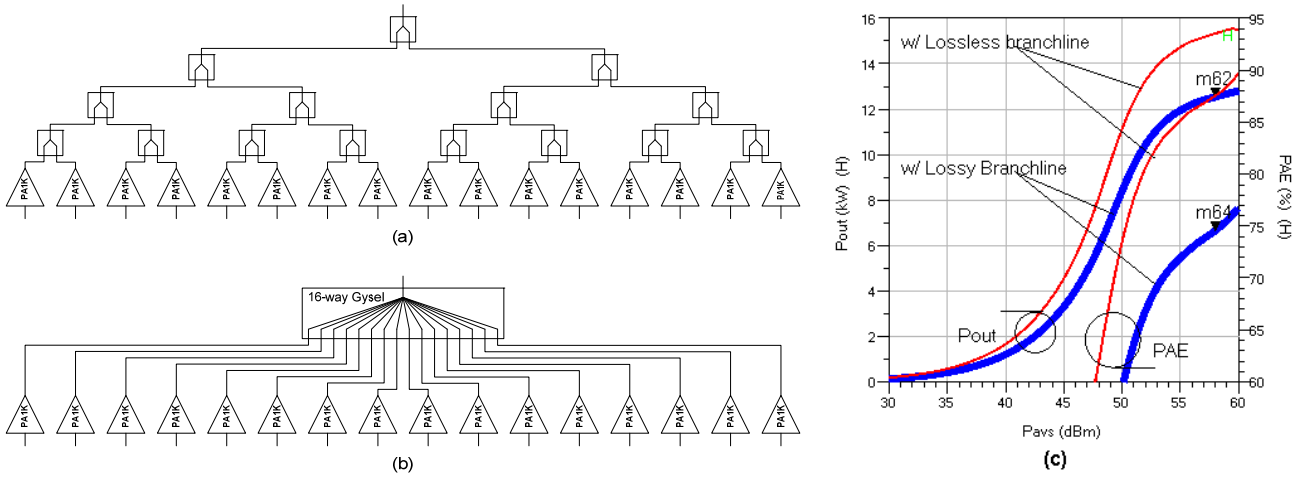
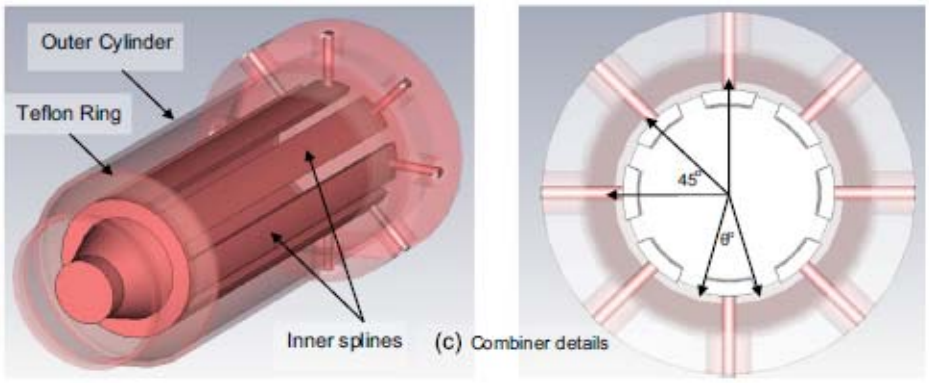


Fig. 8. (a) Multi-level 2-way corporate power combiner (b) single level 16-way combiner scheme and (c) combined output power estimation using T-junctions and Branchline couplers

As a first pass estimate illustrating how the combiner performance impacts the Pout and PAE, we simulate a 12.5 kW amplifier using a multiplicity of QPD1016-based amplifiers and 2:1 branchline combiners in a corporate combining topology (Fig. 7a). The branchline is a reliable and frequently used structure for high power combining [6]. Notice that 16 PA1K units (32 500W transistors) are used instead of the bare minimum of 12.5kW/0.5kW = 25 transistors to account for combiner losses. For a lossless 32:1 power combiner (including the 2:1 combiner inside each PA1K module) the ideal IL due to the power split of each port is 15.051dB. However, a lossy combiner implemented in Rogers 6035HTC 20mil substrate has IL=15.758dB for a 0.707dB circuit loss. This loss is large enough to severely impact Pout and PAE of the overall amplifier as shown in Fig. 7c. From the plot, at Pavs=58dBm, the kW PA with lossy combiner produces Pout=12.537kW, PAE=74.56% while the lossless version produces Pout=15.35kW, 84.762%. Furthermore, the lossless version can theoretically achieve PAE > 80.8% at Pout>13.62kW at Pin>52.5dBm.

These results validate the ability of the 32 QPD1016 amplifiers to achieve >12.5kW but emphasize the importance of the combiner efficiency. Other topologies commonly used in kW amplifiers that should be investigated include the N-way Gysel combiners [28] and Wilkinson combiners which may have lower IL [4]. Because we envision the 12.5kW to be assembled in a rack, the planar Gysel configuration (Fig. 9a) is the most promising. Radial coaxial combiners (Fig. 9b) can be used when combining several racks together for even higher output with low loss [7]. Good isolation is necessary for the main output combiner so that failure of one unit amp does not impact the operation of the others. The input feed network will share its design with the planar output combiner and is less critical to IL.

(a)

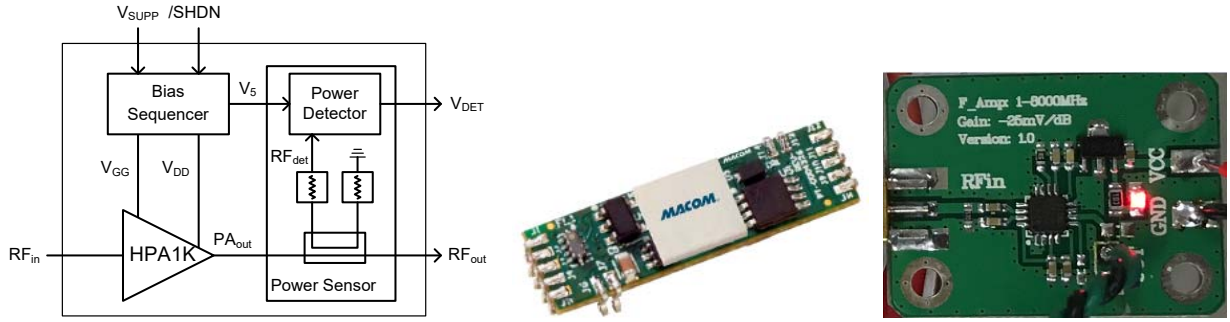


(b)

Fig. 9. (a) Planar 8-way Gysel combiner [4] and (b) radial 8-way Wilkinson combiner [7]

Sequencing and Power Monitoring

Additional subsystems are needed to make the PA1K deployable into a large scale system. These are the bias sequencing and power monitoring subsystems shown in Fig. 10a. One drawback of GaN HEMT devices is that they are FET devices which require negative gate control voltages. Without the proper power-on "sequence" of raising the gate and drain from zero to their required voltages, the devices could experience an undesired operating state or failure. Therefore it is imperative to either design a sequencing circuit [29] or purchase an off the shelf module [30] as shown in Fig. 10b. Power monitoring of the output is important for troubleshooting the PA and identifying failed transistors. Monitoring can be performed using an output directional coupler, attenuator and power detector chip as shown in Fig. 10a fed to a multiplexer bank and a microcontroller. Fortunately, these power detector parts are commercially available (Fig. 10c). Care must be taken to ensure that these circuits to not interfere with the RF operation of the 1kW PA.



(a) (b) (c)

Fig. 10. (a) Unit 1kW amplifier with supporting bias sequencing and power monitoring subsystems (b) MACOM bias sequencer for GaN and [30] (c) Analog Devices RF power detector

Thermal Design

As observed from the PIV curves of Fig. 5, self-heating will severely degrade the IV characteristics of the device and limit the maximum current and voltage swing. The result is reduced RF output power, increased DC dissipated power and lower PAE. Therefore a sensible cooling scheme is needed. In a water-cooled system, each transistor would sit on a baseplate with a water-cooling pipe passing underneath. Coolant can circulated underneath the transistors and to a cooling radiator and fan. Effort is needed to optimize the cooling baseplate, heatsink and coolant distribution network.

RESEARCH POTENTIAL AND FURTHER INQUIRIES

GaN as a replacement for TWT/Klystron application will continue well into the future. The number of opportunities for future research will increase as GaN evolves with the rest of the semiconductor industry.

Echoic Engineering is actively seeking collaboration in the areas of high power GaN for particle accelerators and other applications. Please contact us at www.echoicrf.com or by email at ksyuk@echoicrf.com.

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