A compact 100W, 68% Class F GaN Power Amplifier for L-band GPS

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***Abstract*—The work presents a light weight and compact solid-state power amplifier (SSPA) using GaN technology for L1 band (1.575GHz) GPS applications. Due to immature development of GaN transistor modeling, the PA is designed to operate in Class F mode by using a combination of harmonic load-pull simulations and data-based characterization to achieve high PAE. Additionally, the paper will discuss the solutions to the challenges of thermal management and input matching network design. A hybrid circuit realization achieves Pout=102W, ETA=68% and PAE=66% with gain=15.1dB under 3dB gain compression in CW operation.**

***Keywords*—solid state power amplifiers, GaN HEMT, class F, Global Positioning System, L band, CW.**

I. Introduction

Global Positioning Systems have high requirements on DC power consumption, thermal management, mass and volume of the components, especially for the power amplifier (PA) [1]. Compared with Traveling Wave Tube Amplifiers (TWTAs) conventionally used in satellite systems, GaN based Solid State Power Amplifiers (SSPAs) have much smaller weight and volume. Besides, the combination of several GaN PAs can offer similar output power as a TWTA. Also, switch mode classes or class F techniques can be applied to achieve efficiency levels superior to TWTAs. Therefore, SSPAs are considered possible candidates for TWTAs replacement in space applications. This is particularly true for low frequency bands (from L up to X) where GaN is considered to have some levels of maturity [1]. Especially in L band, GaN devices are generally more efficiently than other materials such as Gallium Arsenide (GaAs).

However, there are also some challenges to design and build a high power GaN PA. With respect to the electrical characteristics of GaN HEMT transistors, they usually require high dc voltage and have high current density, therefore generating high power density. With finite thermal resistances inside the transistor package, the temperature of the transistors increases dramatically, causing the self-heating effect of the transistors. It means the output current decreases as the temperature increases, resulting in degraded performance i.e. lower output power and lower PAE. Therefore, thermal management is very important for high power GaN devices. Additionally, there are two challenges in terms of the design. Due to the immature development of GaN transistor modeling, it's very difficult to apply high efficiency classes such as class F, especially in the situation of lacking a high-accuracy non-linear model. Additionally, it's also very difficult to design input matching network because of the extremely small input impedance of GaN transistors.

The specifications of the project are shown in Table 1. To achieve PAE as high as possible, Class F technique is applied to this design.

Table 1. GaN PA design specifications.

Specifications	Values
Output power	100W
Frequency Range	L1 band: 1.575GHz±12MHz
PAE	60%
Return loss	10dB
Mode	CW

Below, Section II focuses on the application of class F technique by using harmonic load-pull simulation and the design of output and input matching networks. Section III discusses the thermal management, circuit board realization and bias optimization. Section IV presents a conclusion of this work and a discussion for future design.

II. Analysis and Design of a GaN Class F PA

In this project, MACOM NPT2022 is used to design the PA [2]. This transistor is built using GaN-on-Silicon technology. The frequency operating range is from DC To 2GHz. The device operates at 48V and generates output power over 100W in CW operation. The breakdown voltage is 160V which allows a full drain-source voltage swing [2]. The plastic package of the transistor makes it more cost-effective.

A. Class F PA Theory

Like other high efficiency classes, in class F, the overlap between the transient drain voltage and current is minimized so that the DC power dissipation is reduced thereby achieving high efficiency operation. The basic idea of Class F is to apply waveform shaping method. This means the drain current adopts a half-clipped sine waveform, which requires the transistor being biased at around pinch-off voltage. In the meanwhile, the drain voltage adopts a quasi-square waveform. The Fourier series of a square waveform is shown in (1).

$$f_{Square}(t) = \frac{A}{2} + \frac{2A}{\pi}\sum_{n=1}^{\infty}\frac{\sin((2n-1)\omega_0 t)}{2n-1}. \quad (1)$$

where A is the swing of the voltage waveform. Therefore, the voltage waveform consists of dc, fundamental and odd harmonics components. Theoretically, the termination should present short circuit impedances at all of the even harmonics and open circuit impedances at all of the odd harmonics. The corresponding reflection coefficients are $\Gamma_{odd}=1/0^{\circ}$ and $\Gamma_{even}=1/180^{\circ}$, respectively. It's impractical to control an infinite number of harmonics. However, the efficiency of a PA

which is only tuned up to the 3rd harmonic is already very high, 92% theoretically [3].

B. *Harmonic Load-pull Analysis*

Ideal impedances mentioned above, however, only apply to the intrinsic drain of the transistor. Due to the reactances inside the transistor package and inaccessibility to the intrinsic parameters (current and voltage) of the model, waveform shaping method is not feasible in this situation. Therefore, the actual impedances for Class F operation at the extrinsic drain of the transistor need to be resolved. So, harmonic load-pull analysis (shown in Fig. 1) is necessary here to find the optimal impedances. The harmonic-load pull simulations are conducted with the transistor gate terminated in a 50Ω source impedance. In this condition, the transistor is biased around pinch off voltage (Ids=60mA, Vds=50V). An idealized triplexer model perfectly separates the signal path for each harmonic frequency. The individual impedance at each branch is tuned until the PA achieves maximum PAE. The necessary reflection coefficients for Class F operation obtained from the harmonic load-pull are $\Gamma'(fo)=0.907/180^{\circ}$, $\Gamma'(2fo)=0.999/182^{\circ}$ and $\Gamma'(3fo)=0.999/212^{\circ}$. The actual impedance for the 2nd harmonic 2fo is nearly a short circuit while that for the 3rd harmonic 3fo deviates from an open circuit. This indicates that the reactances inside the package have a strong influence on the 3fo. Fig. 2 shows the simulated performance of the PA loaded the optimal impedances obtained above. An output power of 51.3dBm and drain efficiency η of 81% are predicted at 3dB gain compression. This high efficiency demonstrates the potential for class F operation.

C. *Output Matching Design*

Fig. 3 shows the synthesized output matching network which realizes similar reflection coefficients obtained from harmonic load-pull analysis. The transmission lines TL1, TL3 and TL5 serve as a single section microstrip matching network for the fundamental frequency fo. TL2 is an open circuited quarter wave length stub at 2fo, so the impedance seen into TL2 at the 2nd harmonic is a short circuit and 2fo is reflected to the drain of the transistor. The microstripline TL1 causes phase shift for the 2fo. Similarly, TL4 is an open circuited quarter wave length stub at the 3fo and the 3fo is reflected to the drain of the transistor. The combination of TL1 and TL3 cause phase shift for the 3fo. Due to the imperfect reflection of the stubs, the magnitude of Γ' is less than 1 and this also causes the change of optimal impedances. The practical reflection coefficients obtained from the matching network are $\Gamma'(fo)=0.900/181^{\circ}$, $\Gamma'(2fo)=0.994/169^{\circ}$ and $\Gamma'(3fo)=0.984/212^{\circ}$.

D. *Input Matching Network Design*

After completing the output matching network design, the next step is to design the input matching network. First, the impedance looking into the gate of the transistor loaded with the output matching network is Zin=0.07+j*2, which is extremely small. Conjugate matching with Zin brings better return loss and larger gain of a PA. However, it's very difficult to realize this since Zin is very small. Therefore, a small resistance of 0.2Ω is added at the gate of the transistor for matching. Additionally, a resistance can also help increase the stability of the PA. Then two series microstrpline and a shunt capacitor are used for input matching as shown in Fig. 4.

E. *Overall Schematic and Performance*

The overall GaN HEMT Class F PA schematic is shown in Fig. 5. The PA achieves return loss of 11dB. The overall performance is shown in Fig. 6. Since the gain is very high, the curves of ETA and PAE fall on top of each other. At 3dB gain compression, the output power is 51dBm while ETA and PAE are similar and equal to 79% with the gain of 19.6dB.

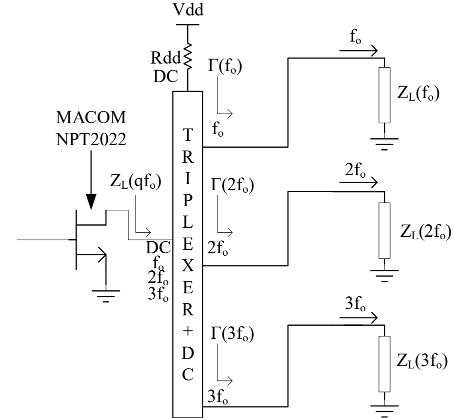

Fig. 1. Harmonic load-pull simulation concept tuned up to the 3rd harmonics.

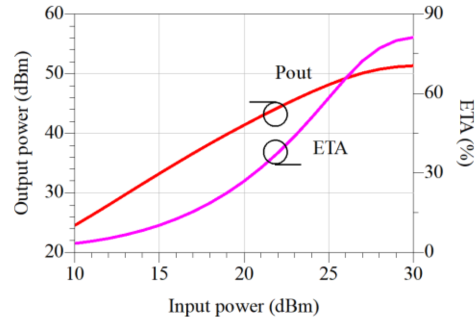

Fig. 2. Performance of the PA applying the optimal impedances obtained from harmonic load-pull analysis.

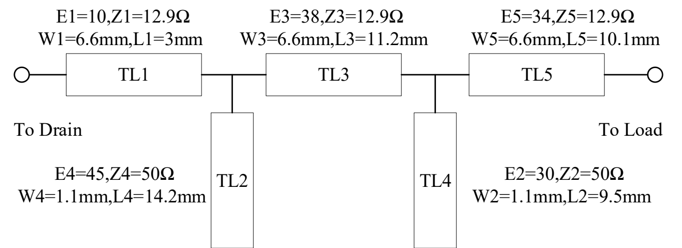

Fig. 3. The output matching network synthesized based on the optimal impedances obtained from harmonic load-pull analysis.

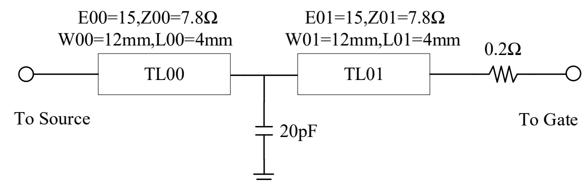

Fig. 4. The input matching network for the GaN PA.

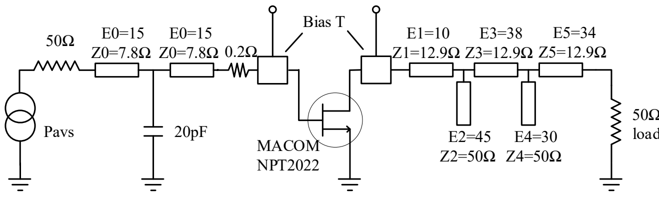

Fig. 5. The overall GaN HEMT Class F PA design.

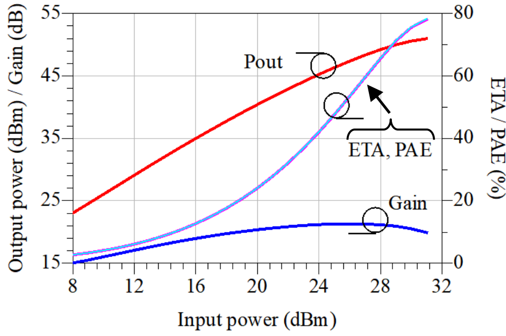

Fig. 6. Pout, Gain, ETA (η) and PAE of the PA applying the optimal impedances obtained from harmonic load-pull simulation.

III. Realization and Performance of PA

A. Circuit Board and Thermal Management

The actual transistor MACOM NPT2022 is implemented in the final hybrid circuit board shown in Fig. 7. The transistor is biased at the same current and voltage as discussed in the simulation, which is (Ids=60mA, Vds=50V). External bias Tees are connected to both ends of the SMA connectors. Notice that the area of the input matching network is very small, so the actual size of the circuit board can be even smaller than the size of the copper base plate, 38×67 mm^2.

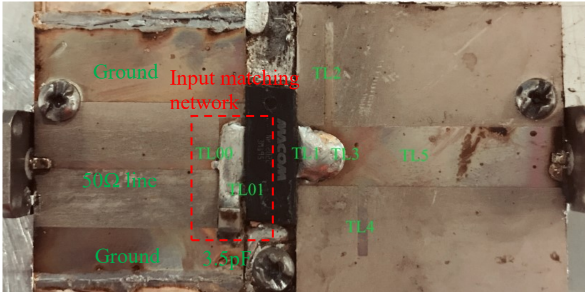

Fig. 7. The realized hybrid Circuit board with the size of 38×67 mm^2.

To help dissipate the heat generated by the transistor, good thermal management is necessary to prevent premature failure, good thermal management is very important. The circuit board used is Rogers 6035HTC which has good thermal conductivity equal to 1.44W/m/K, which is 2.4 times higher than other Rogers laminates [4]. An amplifier test fixture capable of handling over 200W is developed, consisting of a copper base plate and a 500W aluminium heat sink. This test fixture ensures the case temperature to be less than 28°C.

B. Circuit Optimization

Due to immature development of GaN transistor modeling, some circuit tuning and optimization was necessary before the realization of the final board shown in Fig. 7, This includes input and output matching network tuning and bias optimization. The goal of the input matching network tuning was to maximize the return loss above 10dB at 1.575GHz. The actual input matching network doesn't include a resistor due to larger measured input impedance of the transistor loaded with the output matching network.

To tune the output matching network, the first step was to build the network designed in simulation for the fo, and then tune it for maximum PAE of the PA on power test bench. Then the 2fo and 3fo stubs are added and tuned separately also for maximum PAE. For further discussion of harmonic tuning refers to [5]. The optimal impedance at each harmonic frequency is measured on the network analyzer. The comparison of the optimal impedances for maximum PAE between simulation and measurement is shown in Fig. 8(b). The phases are different between simulation and measurement for each frequency, especially for the 3fo. This is mainly due to the discrepancies between the model and the actual transistor. The small signal parameters are shown in Fig. 8(a). S21(dB) is centered exactly at 1.575GHz and the 3dB bandwidth is 70MHz, which is large enough for GPS applications. Return loss of the PA at the input and output are 23dB and 17dB respectively, which are also sufficiently large enough in practical applications.

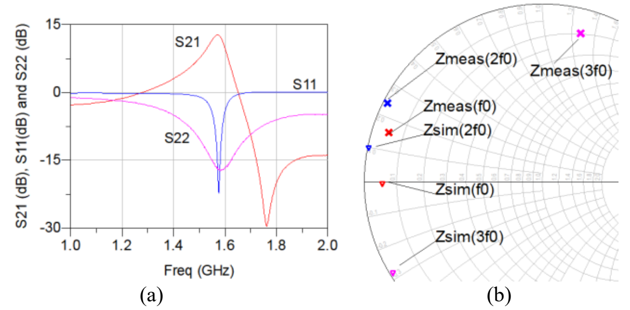

Fig. 8. (a) The small signal parameter of the realized hybrid PA biased at (Ids=60mA, Vds=50V); (b) The comparison of the optimal impedances for maximum PAE between simulation and measurement.

For bias optimization, biases around pinch-off voltage are swept from -1.6V to -1.32V. PAE and Pout at 3dB gain compression are shown in Fig. 9(a) while the gain for full power sweep is shown in Fig. 9(b). As the gate bias is increased, output power is almost same and PAE slightly decreases while linearity is better as seen in the figure. Therefore, the bias is selected to provide better linearity and relatively high PAE while meeting the requirement on 100W output power. The best gate bias is found to be -1.35V, corresponding to the current bias equal to 80mA, which is still around pinch-off voltage.

C. Realized Performance

The performance of the realized hybrid circuit amplifier is shown in Fig. 10. At 3dB gain compression, output power is 50.1dBm; drain efficiency is 68% and PAE is 66% while the gain is 15.1dB. The harmonic measurement is shown in Fig. 11. The power of the 2fo and 3fo is 45dBc below the power of fo for up to 102W, which indicates good gain linearity.

D. Comparison with Other State of the Art SSPAs

The comparison with other state of the art SSPAs is shown in Table 2. Ref. [6] achieved 80% PAE and is tuned up to the 5th harmonic, but the size of the board is 4 times larger than this work. Among PAs which are tuned up to the 3rd harmonic and has similar size of the board, this work has the highest PAE and drain efficiency.

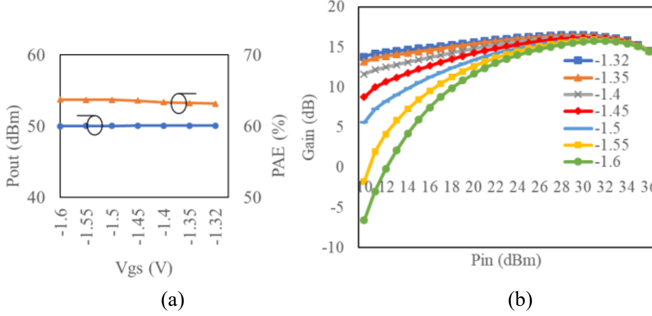

Fig. 9. (a) Pout & PAE vs. gate bias at 3dB gain compression; (b) Gain vs. Pin by varying different gate biases.

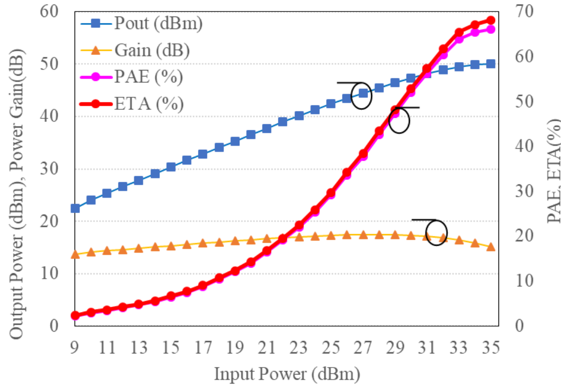

Fig. 10. Pout, Gain, ETA (η) and PAE of the final realized hybrid circuit board.

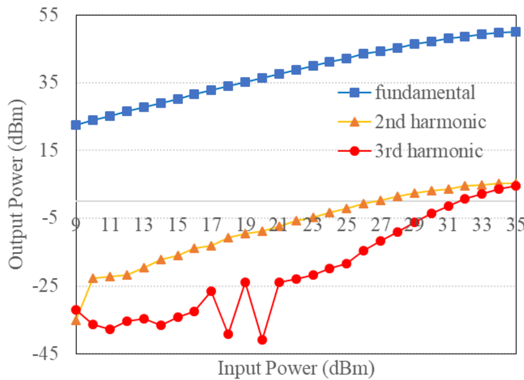

Fig. 11. Measured 2fo and 3fo output power of the hybrid circuit board.

IV. Conclusion & Future Work

A GaN HEMT Class F PA for GPS is designed using a combination of harmonic load-pull simulations and measurement-based technique. The simulation can achieve ETA/PAE= 79% at Pout=51dBm. The realized prototype GaN PA achieves ETA=68%, PAE=66% at Pout=50.1dBm. The 3dB bandwidth is 70MHz and the return loss is 23dB, which are sufficiently large enough to meet the specifications.

The future work of this project would be further improvement for PAE, footprint reduction by replacing part of the microstripline with some capacitors, biasing network design, and wideband operating frequency covering both L1 and L2 bands.

Table 2. State of the art 100W-class CW GaN HEMT PAs in L band.

Ref.	Freq. [GHz]	Pout [W]	Mode	Gain [dB]	PAE [%]	Efficiency [%]	Size [mm×mm]
[6]*	1.2-1.32	140	CW	11	60	N/A	39×25
[7]**	1.3	125	CW	14	77	80	76×152
[8]*	1.575	100	CW	19	N/A	60	N/A
[9]*	1.575	140	CW	13	61	N/A	40×50
T. W.*	1.575	100	CW	15	66	68	38×67

* harmonic is tuned up to the 3rd.
** harmonic is tuned up to the 5th.

Acknowledgment

The authors would like to thank Can Cui for her assistance in the lab and thank Tran Hung for fabricating some of the circuit boards. The authors also would like to thank Dr. Alexei Smirnov, Radiabeam Technologies, Santa Monica, CA for his guidance, transistor contributions and support of this work.

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