High Power Class F GaN HEMT Power Amplifier in L band for Global Positioning Systems Application

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***Abstract*—An L-band high power and high efficiency solid-state power amplifier (SSPA) design is presented. This compact, lightweight GaN HEMT SSPA is designed for nano-satellite GPS applications. This paper focuses on class F to achieve high efficiency by using waveform shaping methods. The optimal magnitude and phase of the fundamental, second and third harmonics (fo, 2fo and 3fo) are optimized by harmonic load-pull to produce a half-rectified sine wave for the drain current and a square wave for the drain voltage. To realize the design, a low impedance transformer with two harmonic traps are implemented by using second and third harmonic open circuit stubs. In CW, the SSPA can achieve 49W of saturated output power with gain of 17.2dB and PAE of 46.2% at 1.575GHz.**

Keywords— SSPA, GaN HEMT, Class F, GPS, L band.

I. INTRODUCTION

Global Positioning System (GPS) and other satellite applications require reliability, high power and efficiency from their power amplifiers (PAs). The PAs should be able to operate at high temperature, generate adequate output power and consume as little DC power as possible. Also, because of the restrictions on weight and volume of the satellite, especially in a nano-satellite, it is of great interest that the PAs can be lighter and smaller while meeting all of the performance specifications [1], [2].

Conventionally, people use Travelling Wave Tube Amplifiers (TWTAs) in satellite systems for their high output power and efficiency. However, due to the drawbacks of a large volume and heavy weight, people are actively investigating solid-state technology as a replacement [3].

GaN technology has made a remarkable breakthrough for its large output power capability [4]. Moreover, the drawbacks that TWTAs have as mentioned above do not exist in GaN technology. Therefore, GaN HEMT is being considered as one of the good candidates for satellite applications. In recent years, space-qualified SSPAs capable of producing more than 100W in L, S and C bands have been developed [5] – [7].

In this paper, a miniature SSPA of 23.6mm x 6.4mm dimensions producing 49W output power and high efficiency is presented. In order to achieve high efficiency, switched-mode operation including class F is investigated. Other switched modes such as class D and E sacrifice linearity while class F and inverse class F have been implemented with adequate linearity [8].

Section II discusses how to design the class F circuit and provides the simulation results produced in Keysight ADS. Section III presents the implementation of the PA and its performance in comparison with other work. Section IV concludes this work.

II. GaN HEMT CLASS F AMPLIFIER DESIGN

The PA design implements the GaN-on-Si HEMT D-Mode transistor, MACOM NPT2024 using a 0.5μm HEMT process [9]. This device operates at 50V and supports CW operation with output levels up to 200W. It is ideally suited for defense communications, land mobile radio, avionic, wireless infrastructure, ISM application and VHF/UHF/L/S band radar [9]. There are two transistors NPT2022 inside a NPT2024 package. The NPT2022 has similar characteristics to those of the NPT2024 except that it generates half of the power or 100W [10]. This design only uses a single NPT2022.

A. Class F Theory

The amplifier design includes input/output matching networks and bias networks at the gate and drain. Figure 1 shows a proposed method using a harmonically-tuned class F amplifier circuit. The input matching network uses a low impedance single section transformer while the output matching network has two stubs to control 2fo and 3fo. RF chokes are used at the VGG and VDD terminals to prevent shorting of the RF power to the DC supplies.

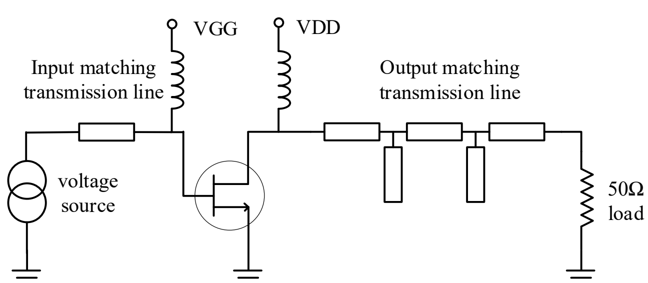

Fig. 1. A class F amplifier circuit with the input and output matching transmission lines, where the output matching network provides optimal impedances at fo, 2fo and 3fo.

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To design a class F amplifier, the output RF signal is shaped such that the current and voltage waveforms at the drain have minimum overlap. Under this condition, the dissipated power consumption will be minimal. Specifically, the amplifier needs to be biased at the pinch-off voltage so that the drain current achieves a half-clipped sine wave. The pinch-off voltage of the device is about -1.7V, but -1.6V is chosen to obtain a flatter gain curve over the input dynamic range. The output matching network is designed to shape the voltage into a square wave. Fourier analysis is given below to show the coefficients of the harmonics [11]

$$f_{half\,\sin}(t)=\frac{A}{\pi}\sin\omega_0 t-\frac{2A}{\pi}\sum_{n=1}^{\infty}\frac{\cos(2n\omega_0 t)}{4n^2-1} \qquad (1)$$

$$f_{square}(t)=\frac{A}{2}+\frac{2A}{\pi}\sum_{n=1}^{\infty}\frac{\sin((2n-1)\omega_0 t)}{2n-1}. \qquad (2)$$

From (1) and (2) above, the half-rectified sine wave has only even harmonics while the square wave has only odd harmonics. Figure 2 shows the current closely resembling a half-rectified sine while the voltage approximating a square wave since harmonic manipulation is limited to 3fo in this paper. To achieve this in a real design, the output matching network should provide a short circuit to 2fo and an open circuit to 3fo.

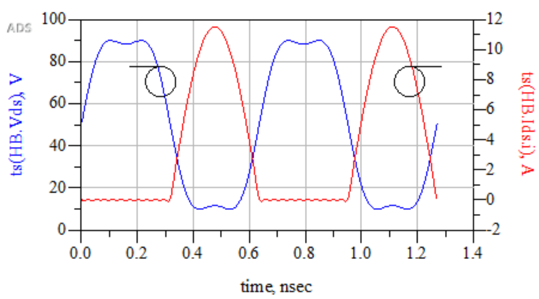


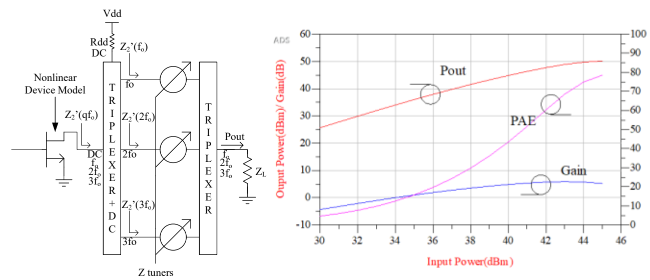
Fig. 2. Ideal class F half-rectified sine wave current and square-wave voltage with up to 3fo manipulation.

B. *Harmonic Loadpull & Matching Network*

Due to the reactances inside the package, the output impedances of the transistor are complex over frequency. Hence, output matching networks should be designed to compensate these reactances, resulting in impedances which deviate from ideal. The harmonic load-pull method is used in simulation to find the optimal impedances at fo, 2fo and 3fo as shown in Fig. 3(a). The triplexer in Fig. 3(a) is only a conceptual simulation tool to separate the harmonic path so that the optimal load can be found for each frequency. Furthermore, the magnitude and phase of the impedance for fo and the input power are swept to achieve a full swing half rectified sine wave. The $|\Gamma|=0.999$ seen by 2fo and 3fo is realized using reflectors while the phases of the impedances for 2fo and 3fo are swept until the proper waveforms of Fig. 2 are attained. Under those conditions, the maximum output power and efficiency can be achieved. The resulting Γs are $\Gamma(fo)=0.869/179^\circ$, $\Gamma(2fo)=0.999/-153^\circ$ and $\Gamma(3fo)=0.999/-145^\circ$.

A single network is synthesized to realize these harmonic impedances. A series TL matching network with two shunt stubs is implemented as shown in Fig. 4. The stub TL2 with electrical length E2 (30°) is designed as an open circuit for the 3fo. A length of 30° at the fundamental frequency is equivalent to 90° at 3fo, resulting in an 3fo open circuit. Similarly, the stub TL4 is designed to be a short circuit for 2fo. TL1, TL3 and TL5 comprise a series impedance transformer with a low characteristic impedance and are designed to give an optimal impedance for fo.

The simulated results while using the synthesized network is shown in Fig. 3(b). Output power = +50dBm, PAE = 78.5% and Gain=5dB is achieved at the saturated power level while the available input power is 45dBm.



(a) (b)

Fig. 3. (a) The harmonic load pull concept showing three impedance tuners for up to 3fo manipulation; (b) The simulated Pout, PAE and Gain for class F amplifier biased at pinch-off voltage by harmonic load pull.

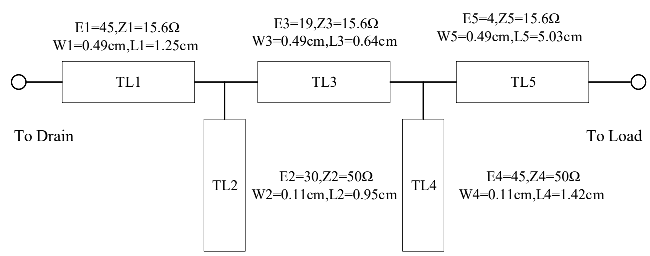


Fig. 4. Output matching network with shunt stub realizations for a short 2fo and an open 3fo.

C. *The Influence of Phase on PA Performance*

To provide a more complete understanding of how the reflector phase offset affects P_{out}, P_{DC} and PAE, the figures of merit vs. the phase of 2fo under multiple input powers is plotted in Fig. 5.

At the low input power range, the phase of 2fo does not influence the PA performance. However, at higher input power, the phase of 205° provides the best P_{out} to P_{DC} and therefore is the best phase offset for PAE optimization.

III. Amplifier Implementation and Performance

The GaN HEMT PA design is implemented on Rogers 6035HTC board, which has thermal conductivity = 1.44W/m/K and reduces the substrate temperature for high power applications [12]. This design implements only one stub in the output network. Fig. 6 shows the test board for the NPT2022 design. The transistor is mounted on the copper baseplate. External bias Ts are used in the prototype.

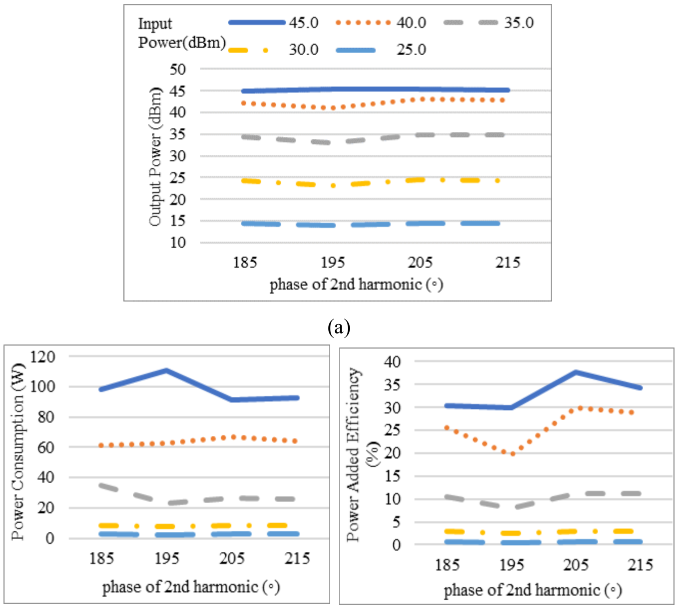


Fig. 5. Simulated (a)output power P_{out}, (b)power consumption PDC and (c)Power Added Efficiency PAE vs. phases of 2^{nd} harmonic with different input power levels.

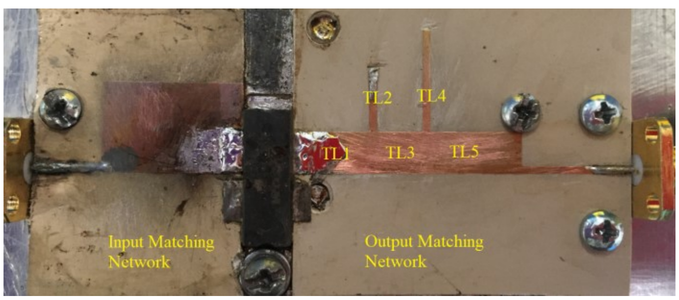


Fig. 6. The class F circuit implementation using the input matching network of one impedance transformer and the output matching network of one transmission line with two stubs only with the NPT2022.

A. *The Influence of Phase on PA Performance*

Since the model has some discrepancies with the actual transistor, an empirical method of evaluating the matching networks with different values of the 2^{nd} order reflector phase offset is needed. The investigation of the phase offset's effect on P_{out}, P_{DC} and PAE is shown in Fig 7.

The PA performance changes slightly with different phases, but it can still be observed that P_{DC} is smaller with a larger Pout and PAE at the phase of 196°. By using a similar technique to test different phases, the optimal phase of the 3^{rd} order reflector can be found at 216°.

B. *Measurements*

The measured Pout, PAE and Gain are shown in Fig. 8(a). At its peak performance, P_{out}=46.9dBm, PAE=46.2% and Gain=17.2dB is achieved at Pin=29.7dBm. The AM/AM (or the Gain vs Pin) curve is linear and shows only 1dB deviation while the PAE drops significantly at the back-off power. Fig. 8(b) shows the harmonic power, where the power of 2fo and 3fo are < -48dBc from the fo power. The S21 measurement for the PA biased at (-1.6V, 50V) is shown in Fig. 9(a). The center frequency is about 1.6GHz and the small-signal bandwidth is roughly 430MHz.

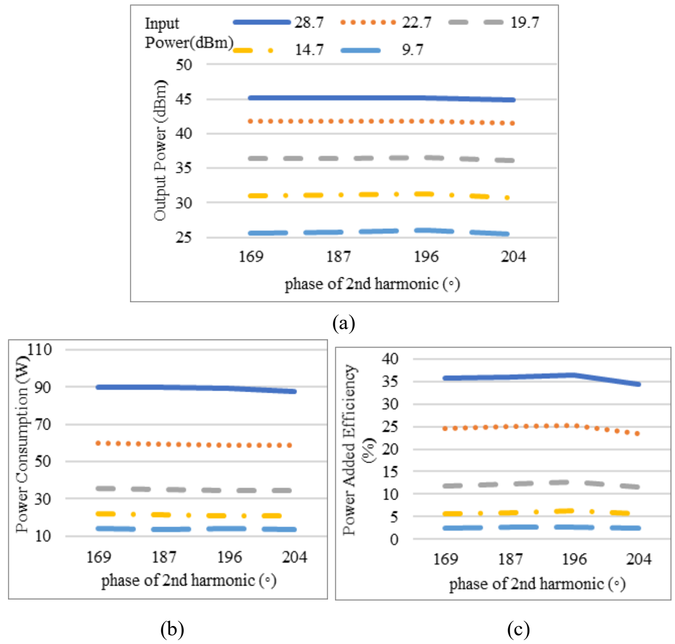


Fig. 7. Measured (a)output power P_{out}, (b)power consumption P_{DC} and (c)PAE vs. phases of 2^{nd} harmonic with different input Power levels.

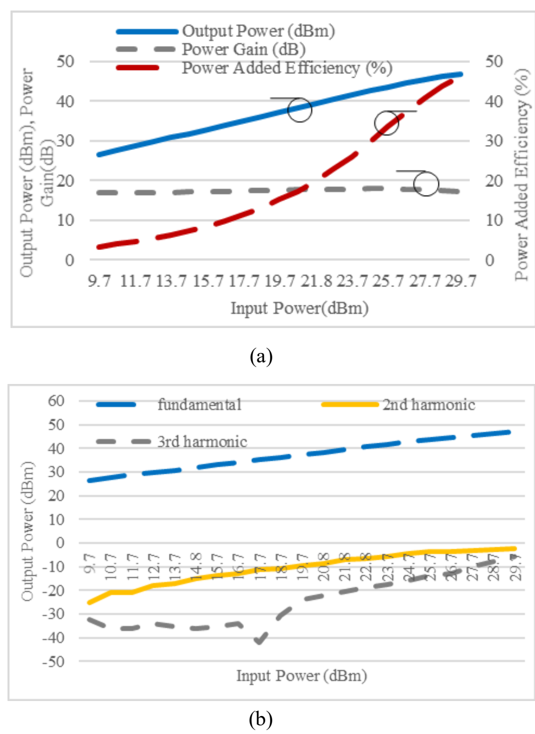
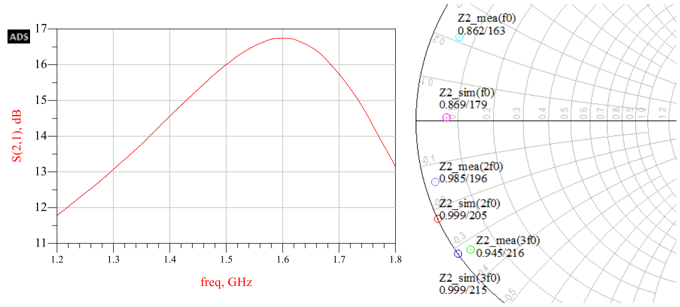


Fig. 8. (a) The measured results of P_{out}, PAE and Gain for class F amplifier biased at a little bit above pinch-off voltage of -1.6V; (b) The output power measured harmonics.



(a) (b)

Fig. 9. (a) The S21 measurements of class F amplifier with roughly 430MHz bandwidth; (b) The measured reflection coefficients compared with the simulation.

Finally, the measured reflection coefficients of the output matching network are $\Gamma(fo)=0.862/163^{\circ}$, $\Gamma(2fo)=0.985/196^{\circ}$ and $\Gamma(3fo)=0.945/216^{\circ}$ shown in Fig. 9 (b). The magnitudes of $\Gamma(fo)$ for simulation and measurement are very close. The magnitudes of $\Gamma(2fo)$ and $\Gamma(3fo)$ are not perfectly 0.999 due to the practical implementation of harmonic reflectors. One explanation for this phase difference can be attributed to discrepancies between the model and the real transistor. Another source of the error can be found in the fabrication and assembly process.

C. *Comparison with other GaN SSPAs*

Table I compares several state-of-the-art GaN PAs for L band. Although the current design is not superior than other work, it still indicates the performance gains that can be achieved using 2fo and 3fo harmonic traps. To realize the maximum benefit of the harmonic traps, we aim to drive additional power into the PA to achieve the saturated output power.

TABLE I. STATE OF THE ART GAN POWER AMPLIFIER FOR L BAND

Ref.	Freq. [GHz]	Pout [W]	Mode	Gain [dB]	PAE [%]	Efficiency [%]
[5]	3.7-4.2	100	CW	15	50	N/A
[8]	1.3	125	CW	14	77	80
[13]	1.575	100	CW	19	N/A	60
[14]	1.2-1.32	140	CW	11	55	60
T. W.	1.575	49	CW	17.2	46.2	47

IV. CONCLUSION

A class F GaN HEMT SSPA for L band GPS applications has been presented. The developed SSPA delivers an output power of 49W with gain of 17.2dB and PAE of 46.2% respectively. Additionally, the authors are still investigating a means to improve the performance. We aim to meet the goal of 100W output power and over 70% PAE, which will be an achievement for a small package device. Such a SSPA will generate power on par with other SSPAs for satellite use [4]–[6].

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