A High Power Inverse Class-F GaN Amplifier for L-band GPS Applications

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***Abstract*— This paper describes a high output power (133W) inverse class-F (class-F^{-1}) GaN HEMT power amplifier (PA) for space applications. The PA operates at 1.227GHz-the L2C second civilian GPS signal operation frequency. Harmonic controlling matching networks are designed to achieve class-F^{-1} current and voltage waveforms at the intrinsic drain. High efficiency is achieved by using harmonic source and load-pull tuning to design the input and output matching networks. The fo matching is performed using a low-Z single-section transformer. Harmonic terminations for 2fo and 3fo are realized using shunt transmission lines placed at optimal offsets from the drain. These matching networks are fine-tuned using a network analyzer. The overall PA performance was tested under different DC biases with swept input power. The best performance is achieved with a bias of V_{ds}=50V, V_{gs}=-3V and P_{in}=32dBm where the PA exhibits 133W output at 42% power-added efficiency (PAE) .**

Keywords*— *GaN HEMT, High Power Amplifier, Inverse Class-F, space application, L-band, GPS-L2C band.

I. INTRODUCTION

Gallium nitride (GaN) technology is one of the most promising technologies for next-generation space applications due to its high breakdown voltage, low thermal conductivity and high current capacity. The unique attributes of GaN such as self-heating, charge trapping, field-plate design and transconductance impact the operating frequency, power, efficiency (PAE), linearity, ruggedness, and transient performance. GaN as the next generation PA technology will replace GaAs solid-state PAs (SSPAs) and traveling wave tube amplifiers (TWTAs). The desire for high density power and good reliability under thermal stress will be satisfied by GaN in ways that existing GaAs FET solutions cannot. Even though TWTAs are the most common amplifier found in space applications that require over 100W output power, GaN SSPAs are gradually replacing them due to the disadvantages of high-voltage power supplies, large size and weight [1].

In our design, the operation frequency is f_o=1.227GHz which is also known as L2 or L2C and serves as the second civilian broadcast frequency for Global Position System (GPS) satellite. Compared with L1C/A (1.575GHz) L2C boosts the accuracy of navigation and provides a signal with improved acquisition [2] and better positioning characteristics [3].

Based on the high power and high efficiency requirements we choose the CGHV14250 GaN high electron mobility transistor (HEMT) device in our design. According to the simulated results, by using properly designed input and output matching networks, we can achieve over +54dBm output power with 83% PAE at 1.227GHz. In the following sections, we report the device characteristics in section II, the class-F^{-1} PA design methodology in section III, and the circuit design, simulation and measurement results in section IV. In the conclusion, we summarize the overall PA performance and also address the various challenges encountered during testing.

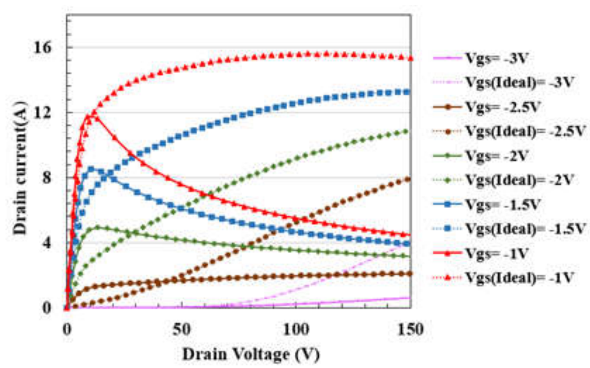

Fig. 1. Simulated IV characteristics of the CGHV14250 with the self-heating model turned on and off.

II. DEVICE CHARACTERISTICS

In our hybrid PA design, we use the CGHV14250 GaN HEMT device from Wolfspeed. It is a commercially available transistor operating in 1.2GHz to 1.4GHz L-band making it suitable for L-Band GPS satellite PA [4]. Although this transistor is designed for over 200W pulsed operation, we will be applying it for use in continuous wave (CW) operation. This presents several unique challenges and will test the capabilities of the device especially its thermal and ruggedness characteristics.

A. Quiescent bias point

Figure 1 shows two sets of simulated IV characteristics at different quiescent gate biases (V_{gs}), with and without (ideal)

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self-heating turned on in the ADS model. From the plot we can observe the impact of self-heating on I_{ds} and select an optimal quiescent bias point for CW operation. One of the requirements for a high power PA is to maximize the current and voltage swing. Ideally, we should choose half of the breakdown voltage, V_b=125V [4] for V_{ds} to achieve a large voltage swing. In reality, we want to minimize the possibility of operating near the breakdown region. Therefore, we pick a value lower than half of V_b to eliminate the chance of over driving the transistor. At the same time, V_{ds} cannot be too low, otherwise the transistor may swing into the triode region. After simulating, we pick a quiescent bias at V_{ds}= 50V and V_{ds}=-3V, the pinch-off voltage [4].

Load line theory provides an the initial approach to estimating the optimal load impedance, R_{opt}. This is pursued by drawing a line from the highest I_{ds} to the quiescent point; and from the slope of this line, R_{opt} can be extracted. The load line princple is only valid for a single bias point. From Fig. 1, a load line at V_{ds}=50V, V_{gs}=-3V gives R_{opt}=6.47Ω. Further investigation of the optimum load is performed using load-pull contours.

B. Load-pull simulation

In order to investigate the performance of CGHV14250 in the frequency domain, we use load-pull simulations in ADS to plot the contours of power delivered to the load (P_{out}) and PAE on the Smith Chart. In the load-pull simulation, we bias the transistor in class-B operation at V_{ds}=5V, V_{gs}=-3V and terminate all higher order harmonics in 50 Ohm. We pick our optimal load on an intersecting point of chosen P_{out} and PAE contours shown in Fig.2. The estimated load impedance represented by the reflection coefficient Γ=0.951 ∠ 162°. The corresponding Z_{Load} provides the highest PAE and output power (P_{out}) at 73.1% and 53dBm, respectively.

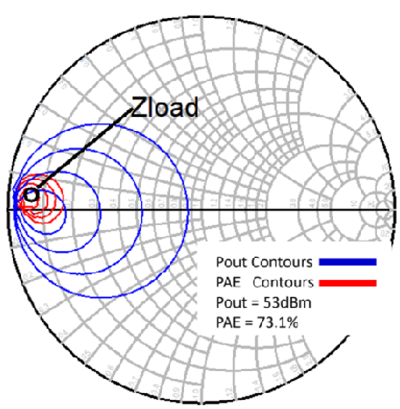


Fig. 2. Load pull simulation with P_{out}, PAE contours and Z_{load} bias at V_{ds}=50V,V_{gs}=-3V.

III. CLASS-F^{-1} PA DESIGN METHODOLOGY

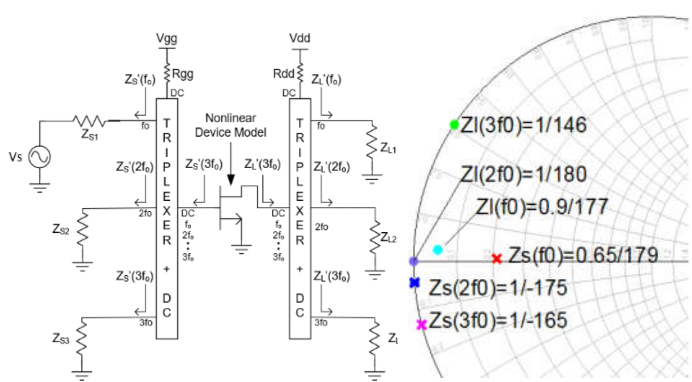
A. Class-F and class-F^{-1} PA operation

Amplifier efficiency can be improved by reducing the power dissipated relative to the P_{out}. For switched-mode PA design, the goal is to eliminate the overlap between drain current and voltage waveforms, which can be done by manipulating the harmonic content of those waveforms. The class-F and class-F^{-1} are high-efficiency power classifications in PA design. The class-F approach uses even harmonics shorts and odd harmonic opens to shape the current into a half-rectified sine wave and the voltage into a square wave.

In class-F^{-1}, the desired waveform shapes for the current and voltage are swapped from the class-F case. Class-F^{-1} has a square-wave current and half-rectified sine wave voltage. The waveform shaping applies the inverse mechanism as the class-F scheme by opening all of the even harmonics and shorting all of the odd harmonics. In the ideal case, if an infinite number of odd or even harmonics have been properly shorted or opened, the voltage waveform and current waveform will have no overlap and a 100% efficiency can be achieved.

B. Practical design methodology

In practical class-F PA realizations, only the first three harmonics are considered, as higher harmonics are naturally shorted through parasitics. In our design, we use harmonic termination analysis to determine the optimum load impedances at the fundamental (f_o), the 2[nd] ($2f_o$) and 3[rd] ($3f_o$) harmonics. The frequency separation is achieved by using an idealized frequency triplexer in ADS at the gate and drain which is shown in Fig. 3(a). The harmonic signal only propagates in the respective frequency path. This is a simulation-based approach to determine the optimum harmonic load impedances.



(a) (b)

Fig. 3. (a) Schematic of triplexer-based harmonic source- and load-pull analysis (b) Resulting source and load impedances derived from the analysis.

During the simulation, the magnitude and phase of Γ_L are designed one-by-one with respect to each harmonic. The design sequence depends on the effective on P_{out} and PAE. We design the $\Gamma_L(f_o)$ parameters first, followed by $\Gamma_L(2f_o)$ then

$\Gamma_L(3f_o)$. After this initial design pass, we will go back to f_o to ensure that the optimal $\Gamma_L(f_o)$ has not shifted due to the application of the harmonic terminations. The purpose is to see if the performance can be improved even further due to high-order harmonic interaction inside the device. Normally, a minor improvement can be achieved. Figure 3 (b) illustrates the values of Γ_S and Γ_L determined from this technique which are labeled as (Zs) and (Z_L), respectively. The complex impedance values are listed in Table 1. By using this method, simulation results showing a P_{out} of +54.6dBm at PAE=81% can be achieved.

TABLE 1. OPTIMAL HARMONIC SOURCE AND LOAD IMPEDANCES

Freq (GHz)	Z_S	Z_L
1.227	10.607+j0.417	2.633+j1.306
2.454	0.003+j2.183	0.003
3.681	0.003-j6.583	0.003+j15.287

IV. MEASURED GAN HEMT PA WITH 133W OUTPUT

A. Circuit design

This circuit design does not include the bias network, we use external bias Ts at both the gate and drain. A majority of the amplifier gain is attained by matching the source at f_o; therefore, matching at $2f_o$ and $3f_o$ is not needed in the input network. In the load matching network, we design the magnitude and phase value for $\Gamma_L(f_o)$, $\Gamma_L(2f_o)$ and $\Gamma_L(3f_o)$ to achieve the highest PAE. All matching networks are fabricated in-house using 20-mil substrate Rogers RO4350B. Figure 4 shows the schematic of the PA.

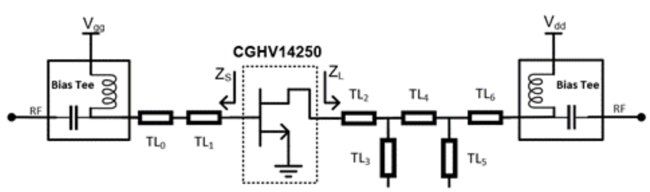


Fig. 4 Circuit schematic of CGHV14250 GAN CW 1.227GHz PA.

The impedance transformer TL_0 andTL_1 at the gate is used to match the S_{11} of the transistor. Lines TL_2, TL_4 and TL_6 at the drain are mainly used to match the f_o impedance to 50 Ohms. The length of these TLs also impacts the harmonic resonator performance of $2f_o$ and $3f_o$. The TL_3 and TL_5 are two shunt stubs employed to resonate the 2nd and 3rd harmonics, respectively. The width and length of the TLs are realized using ADS LineCalc. The simulation is done using harmonic balance and using a set up similar to that used in the previous section. Figure 5 shows the simulated performance of the PA, achieving P_{out}=+54.6 dBm, PAE=81% and Gain=12 dB.

Completion of the impedance matching using a low-Z series-TL transformer at both the input and output resulted in the highest class-F^{-1} performance. To validate the class-F^{-1} operation, the time-domain drain current and voltage waveforms are shown in Fig. 6. It demonstrates a quasi-class-F^{-1} waveform. The drain current waveform resembles a square wave and the voltage resembles a half-rectified sine.

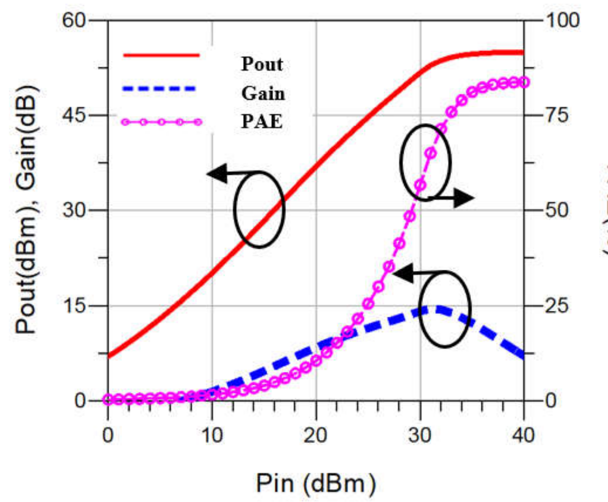


Fig. 5. Power, gain and PAE simulations of the CGHV14250 Class-F^{-1} PA illustrating > 54.6dBm output power, 81% PAE and 12dBm gain.

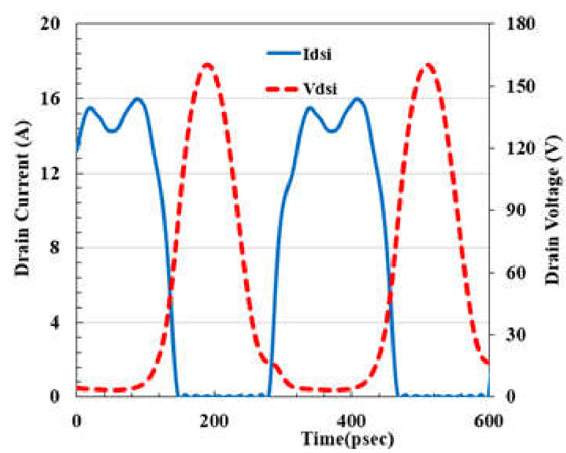


Fig. 6. Time-domain drain waveforms of the CGHV14250 class-F^{-1} PA design.

B. Measurement of the class-F^{-1} PA

To validate the design described in the previous section, the matching networks are realized and the PA is measured at a bias of V_{ds}=50V and V_{gs}=-3V. A max P_{out} of +51 dBm is achieved with a corresponding PAE=42%, and 19 dB gain at 1.227 GHz as shown in Fig. 7. The data shows a trend approaching a 80% PAE peak and 55 dBm saturation power, which is consistent with the simulation. Due to the limitations in the thermal reduction system, measurements at higher output power become very challenging. Without an adequate cooling framework, device reliability is impacted as the output power approaches saturation. Table 2 shows a comparison with recently published high power PAs at L-band against our design [1], [5]-[7].

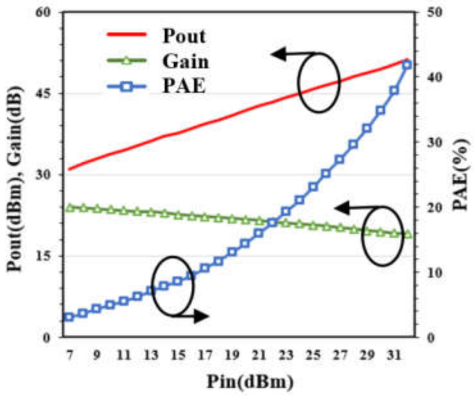


Fig. 7. Measured Power, gain, PAE results of 1.227GHz PA

TABLE 2. STATE OF THE ART GAN PA PERFORMANCE UNDER CW

Ref	Freq. (GHZ)	Pout (W)	PAE (%)	Gain (dB)	Tech.
This Work	1.227	133	42%	19	GaN
[5]	1.91	58	68%	23.998	GaN
[6]	1.30	140	66%	15	GaN
[7]	3.70	>100	67%	~23	GaN
[1]	L-band	>200	60%	~18	TWT

V. CONCLUSION

We design and demonstrate a high efficiency 133 W power amplifier with 42% PAE at 1.227 GHz under CW operation. The transistor used in the design is the Wolfspeed CGHV14250 and the matching networks are fabricated on 20-mil Rogers RO4350B substrate. The PAE can potentially reach 80% at saturated power under improved thermal conditions. The power amplifier has a wide ranging applications in satellite communications, particularly for L-band GPS systems.

One limitation in our measurement is in the thermal reduction setup which makes the case temperature of the transistor very high. The high temperature directly reduces the effective RF output power, thereby decreasing the overall efficiency of the PA. Our next step is to improve the performance of the PA by making more accurate device characterizations and reducing the device operating temperature.

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