An Empirical Large-Signal Model for SiC MESFETs With Self-Heating Thermal Model

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***Abstract*—An empirical large-signal model for high-power microwave silicon-carbide MESFETs capable of predicting self-heating thermal behavior is presented. A generalized drain-current equation based on pulsed-gate *IV* characteristics measuring up to 2 A and 58 V is presented along with its dependence on temperature. A thermal subcircuit with a nonlinear thermal resistance characterized by a dc method is used to model the temperature behavior of the device. The effect of substrate trapping is modeled as a gate–source voltage correction. The complete drain-current model accurately predicts pulsed-gate and pulsed-gate-and-drain *IV* characteristics for various quiescent biases, as well as static *IV* characteristics. The complete large-signal model is shown to accurately predict *S*-parameters, large-signal output, and input reflected power across biases and frequencies, and third-order intermodulation products.**

***Index Terms*—MESFET, model, nonlinear, self-heating, silicon-carbide (SiC), thermal.**

I. Introduction

RESEARCH IN silicon–carbide microwave devices and circuits has been growing rapidly. Devices such as silicon-carbide (SiC) MESFETs are becoming a viable solution to the growing demands of robust high-power microwave applications and have become increasingly competitive with other high-power technologies like GaN. Some of the advantages of SiC MESFETs are its high power density and high drain–source breakdown voltage, making it ideal for high-power applications.

The typical application for SiC MESFETs is in high-power narrowband and broadband amplifiers. A number of SiC MESFET amplifiers have been demonstrated [1] and SiC MESFET amplifiers generating greater than 30 W at high frequencies have been reported [2]. Other circuits that have been developed using SiC MESFETs include mixers and oscillators [3], [4] and this demonstrates the potential to combine high gain and power output with signal-processing functionality. Design of such circuits requires the availability of an accurate large-signal active device model.

Some recent empirical large-signal SiC MESFET models based on the work of Angelov *et al.* [5]–[7] have been reported in [8]–[12]. The model in [8] has shown excellent drain-current and capacitance modeling results. It has also been shown to accurately predict the large-signal power output of a specific amplifier implementation. Models presented in [9]–[11] also accurately predict small-signal performance and power output for lower power GaN and SiC MESFET devices by using a modified Chalmer's model. The work in [12] has demonstrated accurate modeling of both output and input reflected harmonic power for three harmonics by using a simple topology and a single drain-current model based on pulsed-gate-and-drain *IV* characteristics.

One of the challenges in developing a large-signal SiC MESFET model valid over various biases is modeling the self-heating that arises from the high-power nature of the device. Numerous studies have been performed to characterize and model bias-dependent thermal effects by using dynamic *IV* measurements [13]–[18]. Some of the techniques have employed the integration of static biases into drain-current models [13]–[16], while others have characterized thermal behavior of the device [17] and applied changes in temperature directly to circuit model parameters based on dissipated power [9]–[11], [18]. In this study, we employ a combination of these techniques to develop a model that utilizes a well-defined thermal model and trapping correction that accurately predicts pulsed, dc, and RF characteristics over various quiescent biases. It is the authors' opinion that none of the previous work stated has demonstrated such modeling performance over the high-voltage, high-current, and high-power ranges as that presented in this study. The integration of dispersion effects in the model is vital in predicting the large-signal behavior of SiC MESFETs.

This paper presents an empirical large-signal model utilizing Cree Inc.'s CRF-24010 10-W silicon–carbide MESFET [19]. The unmatched SiC MESFET is packaged in a 440166 package with a flange and measures approximately 14.09 mm $\times$ 4.19 mm $\times$ 3.43 mm with a junction to case thermal resistance of 5.6 C/W [19]. A large-signal model for this device is also available from the manufacturer [20], but little technical information about it is known other than it is based on a modified Curtice-cubic model [21]. The model presented in this paper can accurately predict pulsed-gate, pulsed-gate-and-drain, and static *IV* characteristics over a large range of biases by employing a self-heating thermal model and gate–voltage correction that accounts for trapping. The model is also shown to predict the small- and large-signal output and input reflected RF behavior over different biases. The model can also predict RF output and input reflected power over a moderate frequency band, as well as third-order intermodulation products under large-signal drive.

In Section II, the large-signal model is presented. A generalized drain-current model is described and implemented

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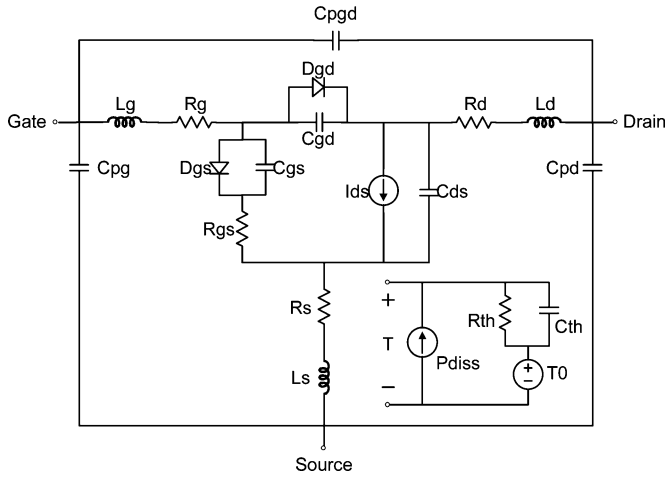

Fig. 1. Large-signal model schematic with self-heating thermal subcircuit.

into a simple large-signal model topology. The thermal model predicting changes in the SiC MESFET junction temperature and its effect on the drain current is described. The gate–source voltage correction accounting for dispersion due to substrate trapping is presented. The complete model including nonlinear current source, small-signal parasitics, nonlinear capacitances, junction diodes, and thermal circuit is implemented in the Agilent ADS software package. In Section III, the fidelity of the model is verified by comparing measured and modeled pulsed-gate and pulsed-gate-and-drain *IV* characteristics under various quiescent bias conditions, as well as static *IV* characteristics. The performance of the model is also verified by comparing model predictions against measured small-signal S-parameters, large-signal harmonics for various biases and against frequency, and third-order intermodulation products. Conclusions are given in Section IV.

II. Model Description

The large-signal model with included thermal subcircuit is shown in Fig. 1.

In all measurements presented here, the SiC MESFET was mounted on an aluminum plate fastened to a heat sink and cooling fan for temperature reduction. The model is seen to be composed of package parasitics and nonlinear elements: $I\mathrm{ds}$, the drain–source current, $D\mathrm{gs}$, the gate–source diode, $D\mathrm{gd}$, the gate–drain diode, $C\mathrm{gs}$, the gate–source capacitance, $C\mathrm{gd}$, the gate–drain capacitance, and the drain–source capacitance, $C\mathrm{ds}$.

A. Large-Signal Drain-Current Modeling

Although the original Chalmers drain-current model [5] assumes separability of $V\mathrm{gs}$ and $V\mathrm{ds}$ terms and straight linear dependencies on $V\mathrm{ds}$, more recent work by the same group has shown a strong interdependence of $I\mathrm{ds}$ parameters on both $V\mathrm{gs}$ and $V\mathrm{ds}$. This appears necessary to accurately model high-power devices that exhibit significant self-heating and current dispersion [9]–[11].

In devices such as high-power SiC MESFETs, it is especially important to model the nonlinear relationships between $I\mathrm{ds}$ and $V\mathrm{gs}$ across the entire range of $V\mathrm{ds}$ in both saturation and linear regimes. Such an expansive fit requires functions of adequate generality, which can be tailored for the particular device of interest. The drain-current model employed in this study is presented in (1) as follows and is a variation of the Chalmers model [5]–[7]:

$$\begin{aligned}
I\mathrm{ds} &= Ipk_{\mathrm{th}}(1+\tanh(\psi)) \\
\psi &= P_1(V\mathrm{gs}_{\mathrm{eff}}-Vpk)+P_2(V\mathrm{gs}_{\mathrm{eff}}-Vpk)^2 \\
&\quad +\cdots+P_N(V\mathrm{gs}_{\mathrm{eff}}-Vpk)^N \\
P_1 &= (Q_{01}+Q_{11}V\mathrm{ds}+\cdots \\
&\quad +Q_{M1}V\mathrm{ds}^M)\tanh(\alpha_{P1}V\mathrm{ds})+P_{10} \\
P_2 &= (Q_{02}+Q_{12}V\mathrm{ds}+\cdots \\
&\quad +Q_{M2}V\mathrm{ds}^M)\tanh(\alpha_{P2}V\mathrm{ds})+P_{20} \\
&\vdots \\
P_N &= (Q_{0N}+Q_{1N}V\mathrm{ds}+\cdots \\
&\quad +Q_{MN}V\mathrm{ds}^M)\tanh(\alpha_{PN}V\mathrm{ds})+P_{N0}. \qquad (1)
\end{aligned}$$

Here, the Pn parameters of the power series describing the $V\mathrm{gs}$ dependence are each a power series expansion of $V\mathrm{ds}$ multiplied by a $\tanh(\alpha\ V\mathrm{ds})$ term and shifted by Pno, the bias independent term of Pn. The parameter Vpk is normally the $V\mathrm{gs}$ value at the peak transconductance $gmpk$. Although $gmpk$ can vary with $V\mathrm{ds}$ in HEMT devices [5], this variation is not strong in SiC MESFETs, except in the low $V\mathrm{ds}$ regime and is accounted for by the use of the Pno and $\tanh(\alpha_{Pn}\ V\mathrm{ds})$ terms for each Pn parameter.

Since the SiC MESFET does not present a bell-shaped transconductance by the same mechanism as in HEMTs, $gmpk$ loses its usual meaning [5]. Therefore, it is necessary to select a certain Vpk such that the drain-current model can be used effectively. For the model presented here, Vpk is chosen at the maximum transconductance point found within the available *IV* dataset, which occurs at $V\mathrm{gs}=0.5$ V, the highest available gate–source bias. The dataset presented here is large and allows the selection of Vpk just below the onset of forward conduction of the gate–source diode. The subsequent Ipk values are defined by the $I\mathrm{ds}$ corresponding to $Vpk=0.5$ V across the $V\mathrm{ds}$ bias range [12]. Although Ipk as a function of $V\mathrm{ds}$ can be table based in the absence of self-heating, it is modeled here using the expression

$$\begin{aligned}
Ipk(T_0) &= (J_3V\mathrm{ds}^3+J_2V\mathrm{ds}^2+J_1V\mathrm{ds}+J_0) \\
&\quad \times \tanh(\alpha_{Ipk}V\mathrm{ds}) \qquad (2)
\end{aligned}$$

where the Jn and α_{Ipk} values are fitting parameters.

In characterizing the SiC MESFET, a multiplicity of pulsed-gate *IV* measurements were taken to obtain the device's performance in the absence of any static self-heating conditions. The *IV* characteristics of the device were measured from $V\mathrm{gs}=-11.0$ V to 0.5 V in 0.5-V steps and $V\mathrm{ds}=0$ V to 58 V in 2-V steps with a quiescent gate bias of $V\mathrm{gsq}=-11.0$ V using a pulsewidth of 100 ns and pulse period of 400 ms. The pulse parameters are carefully chosen here to prevent the onset of dispersion during the pulsed state and sufficient relaxation of the dynamic device behavior between pulses [22].

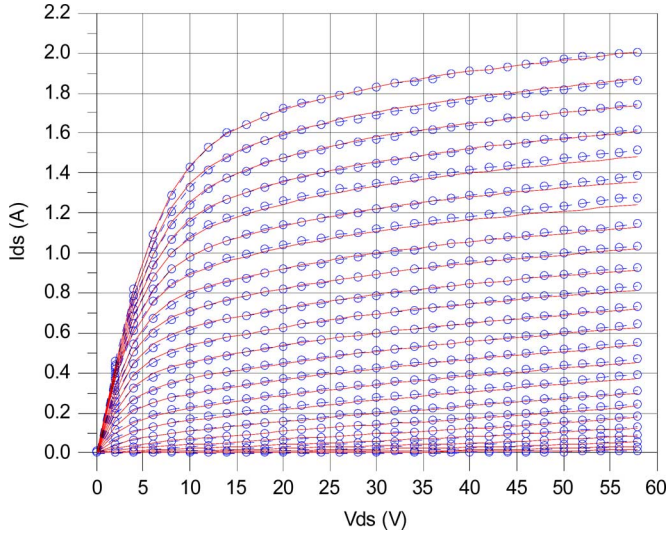

Fig. 2. Pulsed-gate *IV* characteristics at $Vgsq = -11.0$ V, $Vgs = -11.0$ V to 0.5 V in 0.5-V steps, $Vds = 0$ V to 58 V in 2-V steps. Measured (circles) and modeled (solid lines).

TABLE I
PARAMETERS OF DRAIN–SOURCE CURRENT MODEL

Q_{41}	Q_{40}	α_{P4}	P_{4o}
1.3891e-6	-244.43e-6	62.717e-3	-256.11e-6
Q_{31}	Q_{30}	α_{P3}	P_{3o}
-925.45e-9	-607.70e-6	107.26e-3	443.88e-6
Q_{11}	Q_{10}	α_{P1}	P_{1o}
-302.75e-6	172.53e-3	147.32e-3	27.988e-3

The modeled versus measured pulsed-gate *IV* values are shown in Fig. 2. These computed results show that, for a large range of biases, the formulation is extremely effective at modeling the pulsed-gate *IV* characteristics with zero static power dissipation. The parameters used to realize the model are presented in Table I. All other Qnm and Pno parameters are equal to zero.

B. Thermal Modeling and the Effect on Drain Current

It is important to consider the thermal behavior of the device when developing a generalized model since the quiescent bias point will substantially affect its performance. The equivalent-circuit model for the thermal behavior of the device was previously shown in Fig. 1 [8]. This circuit approximates the temperature and thermal charging and discharging of the device according to the expression

$$T = T_0 + \Delta T' = T_0 + \Delta T(1 - \exp(-t/\tau)) \tag{3}$$

where T is the temperature, T_0 is the ambient temperature, $\Delta T = R_{\rm th}P_{\rm diss}$ is the change in temperature, and $\tau = R_{\rm th}C_{\rm th}$ is the thermal time constant.

There exist a number of approaches for extracting the nonlinear thermal resistance $R_{\rm th}$, which relates the junction temperature to the dissipated power [23]–[28]. In the approach used here, $R_{\rm th}$ was extracted from dc forward bias gate–source diode

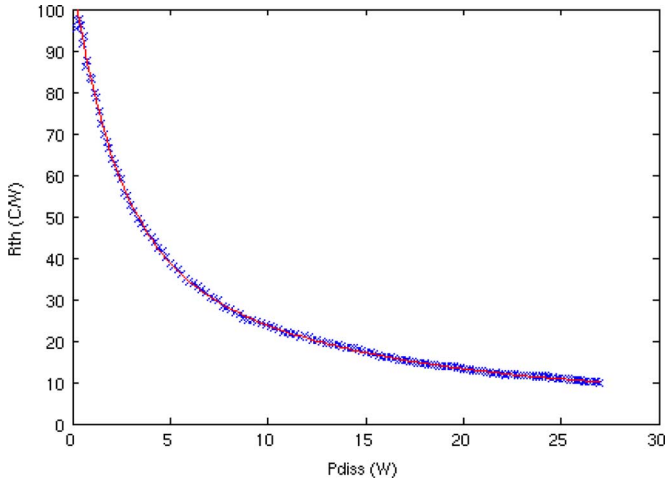

Fig. 3. Thermal resistance $R_{\rm th}$ versus dissipated power up to 27 W. Measured ($\times$) and modeled (solid line).

TABLE II
PARAMETERS OF THERMAL RESISTANCE MODEL

R_2	ϕ_2	R_1	ϕ_1	R_0
41.0187	10.9999	60.1912	2.18674	6.60522

current measurements, which were performed over a range of static drain–source voltages in a manner similar to that in [17] and [23]. The technique provides values for $R_{\rm th}$ characterized over various dissipated powers.

The thermal resistance measured up to 27 W is shown in Fig. 3 and modeled by

$$R_{\rm th}(P_{\rm diss}) = R_2\exp(-P_{\rm diss}/\phi_2) + R_1\exp(-P_{\rm diss}/\phi_1) + R_0 \tag{4}$$

where R_0 is a constant term, R_1 and R_2 are the coefficients of the first and second exponential terms, respectively, and φ_1 and φ_2 are the decay constants of the first and second exponentials, respectively. The extracted model parameters are provided in Table II. The thermal resistance saturates as Pdiss increases due to the saturation of the junction temperature at around 570 K.

Integration of the self-heating effects can be done primarily by modifying the Ipk equation according to the change in temperature in [7]. Here, the temperature-dependent $Ipk_{\rm th}$ is written as

$$Ipk_{\rm th} = Ipk(T) = \frac{Ipk(T_0)}{1 + K_{Ipk}\Delta T'} \tag{5}$$

where $Ipk(T_0)$ is Ipk with no self-heating, $\Delta T'$ is the time-dependent temperature change computed by the thermal circuit, and K_{Ipk} is a fitting parameter. Equation (5) is mathematically equivalent to the relationship presented in [7], but is written in this form to emphasize the fact that Ipk will generally decrease as temperature increases. A bias-dependent term K_{Ipk} is used to satisfy the above equation for all quiescent biases and can

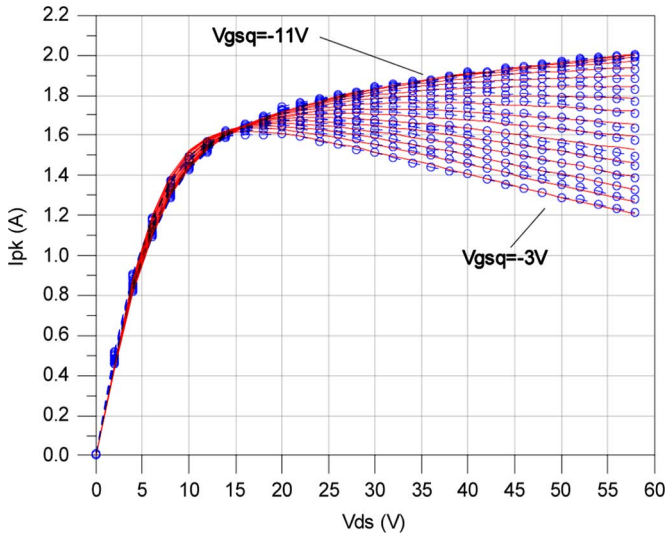

Fig. 4. Ipk versus $V\mathrm{ds}$ for $V\mathrm{gsq} = -11.0$ V to -3.0 V in 0.5-V steps. Measured (∘) and modeled (solid lines).

take the form of a table or an analytical expression. Here, the expression used for K_{Ipk} is

$$\begin{aligned} K_{Ipk} &= K_{Ipk1} V\mathrm{dsq} + K_{Ipk0} \\ K_{Ipkn} &= K_{Ipkn\,\max}(1-(-1)^n \tanh(\psi_{Ipkn})) \\ \psi_{Ipkn} &= C_{n1}(V\mathrm{gsq} - V\mathrm{gsq}_{Ipkn}) \\ &\quad + C_{n3}(V\mathrm{gsq} - V\mathrm{gsq}_{Ipkn})^3, \qquad n = 0, 1 \end{aligned} \tag{6}$$

where $K_{Ipkn}, K_{Ipkn\max}, C_{n1}, C_{n3}$, and $V\mathrm{gsq}_{Ipkn}$ are fitting parameters.

This thermal relationship is applied to Ipk at $Vpk = 0.5$ V for static gate biases of $V\mathrm{gsq} = -11.0$ V to -3.0 V in 0.5-V steps from $V\mathrm{ds} = 0$ V to 58 V in 2-V steps. The resulting Ipk values at these quiescent biases are shown in Fig. 4. Comparing the modeled versus measured data, it is observed that the relationship described by (6) is valid and effective for the modeling of the thermal effects on Ipk.

In addition to Ipk, the Pn parameters will also vary with temperature, though its effect on $I\mathrm{ds}$ as a function of self-heating is not as pronounced as that of Ipk. Pn is modified as a function of temperature using the following relationship [10]:

$$P_{n\mathrm{th}} = P_n(1 + K_{Pn}\Delta T') \tag{7}$$

where K_{Pn} is similar in function as K_{Ipk} described above, but can be formulated using a simpler expression.

The transient change in $I\mathrm{ds}$ from one temperature to another will follow the same exponential temperature response described in (3). Therefore, once R_{th} is known, τ and the thermal capacitance $C\mathrm{th}$ can be approximated from transient pulsed-gate $I\mathrm{ds}$ behavior measured over long pulse durations. A $C\mathrm{th}$ value of 4.20 mF was extracted from a long pulsed-gate transient measurement of $I\mathrm{ds}$ with a pulsewidth of 2 ms for $V\mathrm{gsq} = -11.0$ V pulsed to -3.0 V at $V\mathrm{ds} = 55$ V.

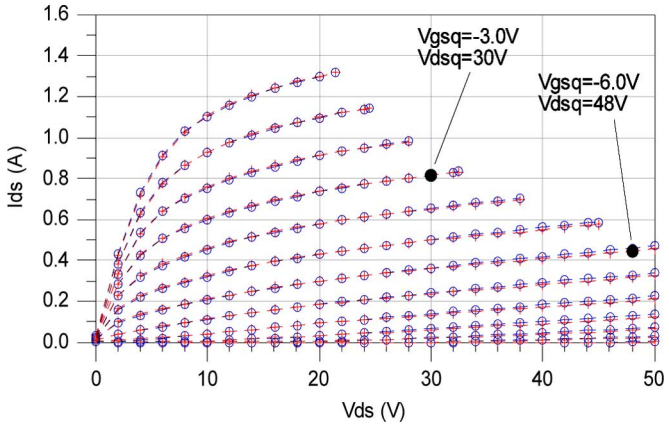

Fig. 5. Comparison between two pulsed-gate-and-drain *IV* measurements. Measurements at quiescent point of $V\mathrm{gsq} = -3.0$ V and $V\mathrm{dsq} = 30$ V (circles) and $V\mathrm{gsq} = -6.0$ V and $V\mathrm{dsq} = 48$ V (crosses). Quiescent points are identified as solid dots.

C. Dispersion Due to Trapping

Pulsed-gate *IV* responses can be used to characterize the thermal behavior of the SiC device using a relatively small number of *IV* datasets. However, pulsed-gate-and-drain *IV* characteristics provide a better prediction of large-signal behavior at a given operating point. To incorporate the effects of steady-state substrate trapping, a gate–source voltage correctional term is incorporated in the drain-current model presented in this paper. This enables the model to accurately predict both pulsed-gate and pulsed-gate-and-drain *IV* characteristics.

It has been shown that dispersion due to traps in SiC MESFETs is due primarily to substrate traps [29], which are the main focus here. A Nanometrics DiVA Dynamic *I–V* Analyzer [30] was used to measure the pulsed-gate-and-drain *IV* characteristics of the SiC MESFET using 200-ns pulses separated by 1 ms. Two sets of pulsed-gate-and-drain *IV* characteristics, one biased at $V\mathrm{gsq} = -3$ V and $V\mathrm{dsq} = 48$ V and the other biased at $V\mathrm{gsq} = -6$ V and $V\mathrm{dsq} = 48$ V are compared in Fig. 5. The device dissipates approximately 25 W at both quiescent biases and shows very similar drain-current characteristics implying that dynamic substrate trapping behavior is not present [29], [31]. This means that only steady-state trapping affects the drain-current performance when using pulse durations of 200 ns or less.

In this study, the effect of steady-state trapping has already been included in the drain-current model derivation based on pulsed-gate *IV* characteristics. Therefore, an adjustment of the effective gate–source voltage based on the pulsed and quiescent drain biases can be formulated by writing

$$V\mathrm{gs}_{\mathrm{eff}} = V\mathrm{gs} + \alpha_{\mathrm{trap}}(V\mathrm{ds} - V\mathrm{dsq}) \tag{8a}$$

and

$$\alpha_{\mathrm{trap}} = \alpha_{\mathrm{trap1}} V\mathrm{dsq} + \alpha_{\mathrm{trap0}} \tag{8b}$$

where $V\mathrm{gs}$ is the instantaneous gate–source voltage, $V\mathrm{ds}$ is the instantaneous drain–source voltage, $V\mathrm{dsq}$ is the quiescent drain–source voltage, and α_{trap0} and α_{trap1} are fitting parameters. Equation (8a) is a modified version of that found in [31] and [32] in that the calculation of the backgate voltage has been

TABLE III
SMALL-SIGNAL PARASITIC PARAMETERS

Rg	Rd	Rs	Cpgd
0.35868 Ω	1.2269 Ω	0.59765 Ω	0.00000 pF
Lg	Ld	Ls	Cpg / Cpd
737.84 pH	673.36 pH	44.700 pH	0.76778 pF

bypassed for a direct computation of the substrate trapping effect on the effective gate–source voltage. Good results can be achieved by making $\alpha_{\rm trap}$ a linear function of the quiescent drain voltage, as shown in (8b).

The comparison of modeled and measured pulsed-gate-and-drain IV characteristics are provided in Section III.

D. Parasitics and Capacitance Modeling

The extrinsic small-signal model parameters are extracted based on standard methods using statically biased S-parameter measurements [33], [34]. The extrinsic capacitances are extracted from pinched field-effect transistor (FET) S-parameters, while the extrinsic inductances and resistances are extracted using cold-FET S-parameter measurements. The parameter values for these parasitics are provided in Table III. The intrinsic device parameters were extracted from hot-FET S-parameter measurements taken with the device biased in the active region for $V{\rm gs}$ values ranging from -10 to -5 V in 1-V steps and $V{\rm ds}$ from 0 to 60 V in 2-V steps. The intrinsic $C{\rm gs}, C{\rm gd}, C{\rm ds}, gm$, and $g{\rm ds}$ are extracted from each set of hot-FET S-parameters and placed in a full small-signal model such that there is good agreement between the measured and modeled responses. The extracted values for the voltage-dependent capacitors $C{\rm gs}, C{\rm gd}$, and $C{\rm ds}$ are then modeled using the Chalmers capacitance model and implemented into Agilent Technologies' Advanced Design System (ADS) in the form of charge equations [7].

E. Diode Modeling

The characteristics of the gate–source and gate–drain diodes in forward conduction are modeled using the standard diode equation. The saturation currents and thermal voltages of the diodes are extracted by measuring the device in forward conduction [35]. These forward conduction gate current measurements are also used to assist in the extraction of the parasitic gate, drain, and source resistances, as described by [35].

III. EXPERIMENTAL MODEL VERIFICATION

In this section, the performance of the drain-current model is compared with measured pulsed-gate *IV* characteristics at four different quiescent gate biases, with pulsed-gate-and-drain *IV* characteristics at three different quiescent biases, and finally with static *IV* characteristics. To validate the RF performance of the model, it is compared with measured S-parameter data to verify the small-signal accuracy, and measured output and input reflected power data for the first three harmonics to verify the large-signal accuracy. The RF performance of the device is measured and modeled at two different biases to exemplify the broad range of validity. Additionally, comparisons with large-signal measurements as a function of frequency and with measurements of third-order intermodulation products obtained from a two-tone test are used to validate the fidelity of the model.

A. Pulsed-Gate IV, Pulsed-Gate-and-Drain IV, and Static IV Characteristics

The pulsed-gate *IV* measurements described in Section II were conducted for quiescent gate biases from $V{\rm gsq} = -11.0$ V to -3.0 V and used for verification of the thermal model and its effect on the drain current. The pulsed behavior of the model is computed using transient simulations and the resulting pulsed-gate *IV* curves for $V{\rm gsq} = -9.0$ V, -7.0 V, -5.0 V, and -3.0 V are given in Figs. 6–9, respectively. According to these results, the large-signal model with thermal circuit is capable of closely reproducing the pulsed-gate *IV* behavior. These curves serve to illustrate the efficacy of the thermal portion of the model. The model modifies the drain current at zero static power dissipation, as was shown in Fig. 2, into the respective drain current at static power dissipations defined by the quiescent bias.

The performance of the model is also validated by comparing pulsed-gate-and-drain *IV* data with model predictions computed using transient simulations. The modeled and measured pulsed-gate-and-drain *IV* characteristics are shown in Figs. 10–12 for quiescent biases at $V{\rm gsq} = 0$ V, $V{\rm dsq} = 0$ V, at $V{\rm gsq} = -3$ V, $V{\rm dsq} = 30$ V, and at $V{\rm gsq} = -6$ V, $V{\rm dsq} = 48$ V, respectively. The results demonstrate that there is good agreement between the model output and measurements. Furthermore, this validates the trapping dispersion relationship developed in Section II in which the effective gate–source voltage modification permits the drain-current model derived from pulsed-gate *IV* characteristics to also predict pulsed-gate-and-drain *IV* characteristics.

In addition to the dynamic *IV* characteristics shown in Figs. 6–12, the model can also predict static *IV* curves. The measured versus modeled static *IV* characteristics from $V{\rm gs} = -11.0$ V to -3.0 V, $V{\rm ds} = 0$ V to 58 V are given in Fig. 13. Again, this demonstrates the validity of the temperature-dependent drain-current model presented in this study.

B. Small-Signal S-Parameters

The S-parameters of Cree Inc.'s SiC MESFET were measured over a range of bias points from $V{\rm gs} = -10$ V to -5 V in 1-V steps for $V{\rm ds} = 0$ V to 60 V in 2-V steps utilizing an HP 8510B vector network analyzer employing a microstrip thru-reflect-line (TRL) calibration from 0.1 to 4.0 GHz. The S-parameters of the model compared with measured data for representative biases of $V{\rm gs} = -10$ V, $V{\rm ds} = 55$ V and $V{\rm gs} = -7$ V, $V{\rm ds} = 55$ V are shown in Fig. 14. An examination of these plots reveals a close agreement between the measured and modeled data, thus verifying the functionality of the model when employed in a small-signal mode.

To achieve good agreement between modeled and measured S-parameters, many large-signal models use two drain-current

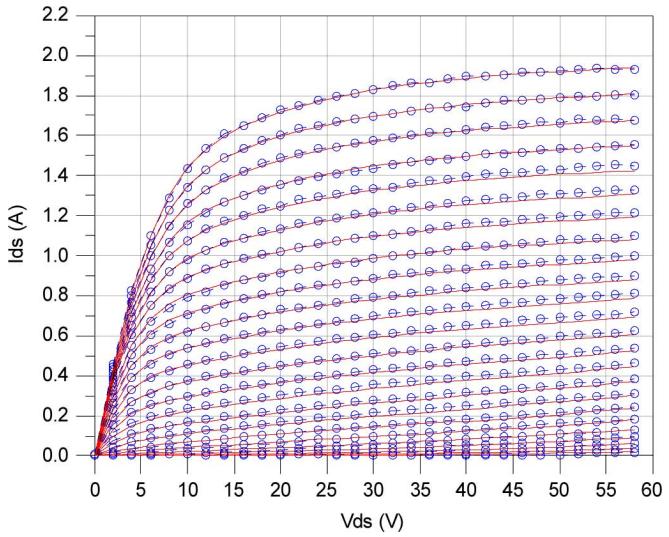

Fig. 6. Pulsed-gate *IV* characteristics at $Vgsq = -9.0$ V, $Vgs = -11.0$ V to 0.5 V in 0.5-V steps, $Vds = 0$ V to 58 V in 2-V steps. Measured ($\circ$) and modeled (solid lines).

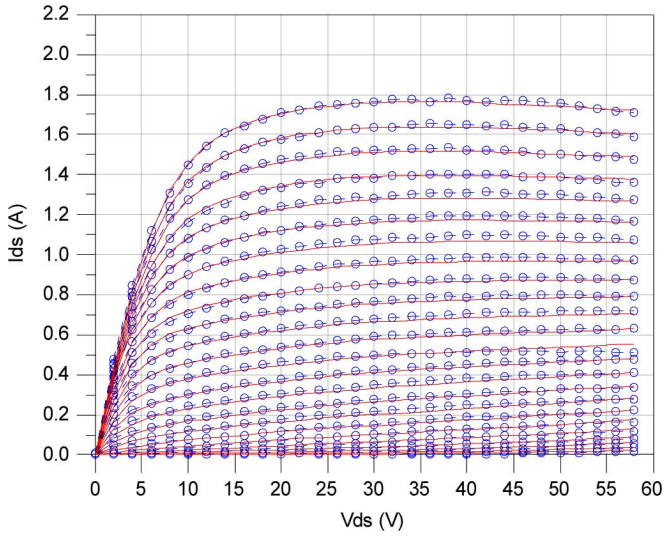

Fig. 7. Pulsed-gate *IV* characteristics at $Vgsq = -7.0$ V, $Vgs = -11.0$ V to 0.5 V in 0.5-V steps, $Vds = 0$ V to 58 V in 2-V steps. Measured ($\circ$) and modeled (solid lines).

sources. One source models the dc drain current and the other operates at RF frequencies to compensate for differences between gm and $g$ds derived at dc and those derived from S-parameters [7]. The RF current source provides supplementary current such that gm and $g$ds are accurate under RF conditions, but this requires additional circuit characterization.

In this model, a single drain-current source based on pulsed-gate *IV* characteristics and adapted for predicting pulsed-gate and pulsed-gate-and-drain *IV* characteristics is used. According to the comparison with S-parameter data, this current source along with appropriately modeled parasitic elements can accurately predict the small-signal behavior of the device without using an RF current generator.

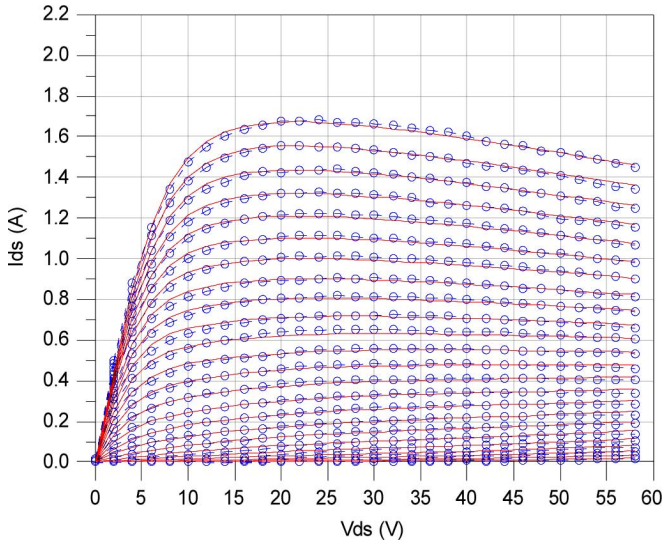

Fig. 8. Pulsed-gate *IV* characteristics at $Vgsq = -5.0$ V, $Vgs = -11.0$ V to 0.5 V in 0.5 V steps, $Vds = 0$ V to 58 V in 2-V steps. Measured ($\circ$) and modeled (solid lines).

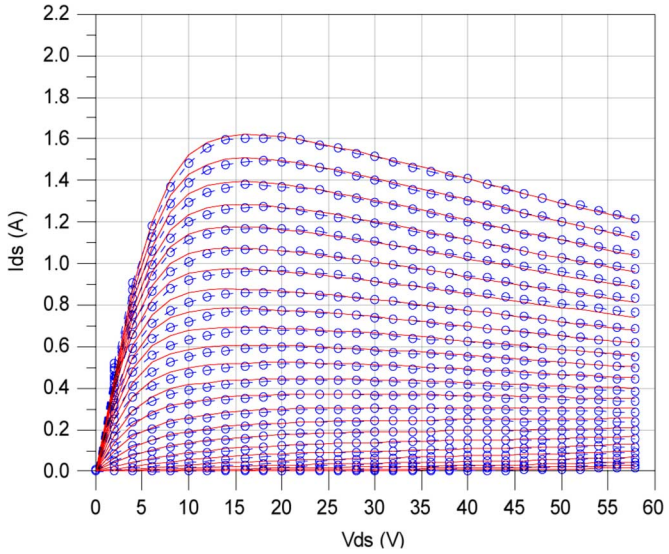

Fig. 9. Pulsed-gate *IV* characteristics for $Vgsq = -3.0$ V, $Vgs = -11.0$ V to 0.5 V in 0.5-V steps, $Vds = 0$ V to 58 V in 2-V steps. Measured (circles) and modeled (solid lines).

C. Output and Input Reflected Harmonic Power Versus Incident Power and Versus Bias

The fidelity of the power performance of the model is verified by comparing its output and input reflected predictions with measured power data. The transmitted output and input reflected power of the device at $fo = 2$ GHz over an available power range from 21 to 40 dBm in 1-dBm steps for two biases, $Vgsq = -10.0$ V, $Vds = 55$ V and $Vgsq = -7.0$ V, $Vds = 55$ V, are simulated and compared with measured data as shown in Figs. 15 and 16, respectively.

According to the output power characteristics shown in Figs. 15 and 16, the model provides a very good prediction of the output power for the first three harmonics for the two representative gate biases. In addition, the input power reflected

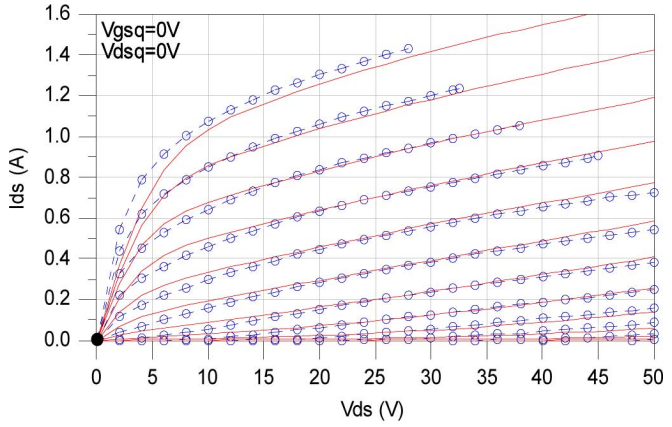

Fig. 10. Pulsed-gate-and-drain *IV* characteristics at $Vgsq = 0$ V, $Vdsq = 0$ V. The bias range is $Vgs = -15.0$ V to -2.0 V in 1-V steps, $Vds = 0$ V to 50 V in 2-V steps. Measured (∘), modeled (solid lines), and quiescent point (dot).

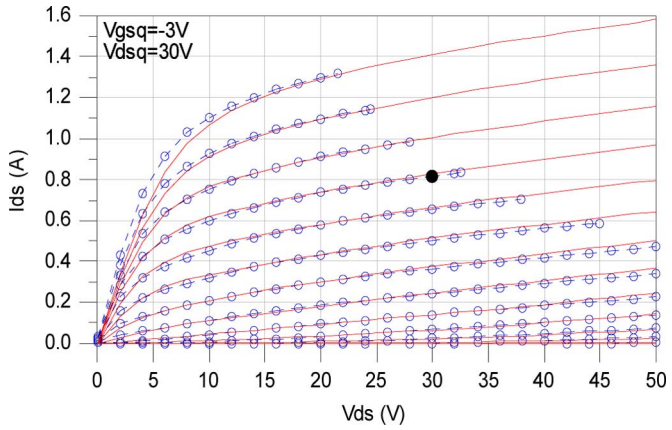

Fig. 11. Pulsed-gate-and-drain *IV* characteristics at $Vgsq = -3$ V, $Vdsq = 48$ V. The bias range is $Vgs = -15.0$ V to 0 V in 1-V steps, $Vds = 0$ V to 50 V in 2-V steps. Measured (∘), modeled (solid lines), and quiescent point (dot).

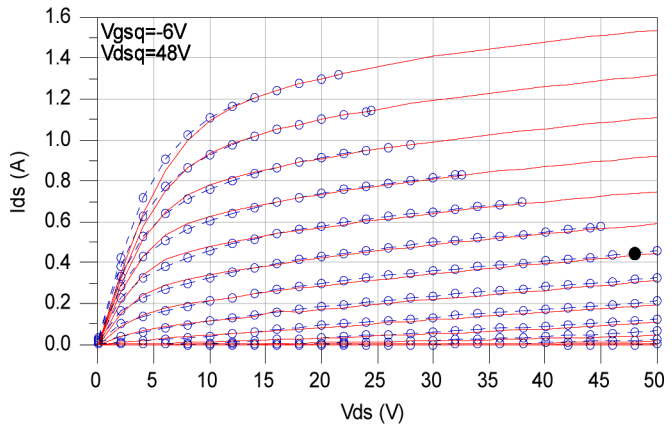

Fig. 12. Pulsed-gate-and-drain *IV* characteristics at $Vgsq = -6$ V, $Vdsq = 48$ V. The bias range is $Vgs = -15.0$ V to 0 V in 1-V steps, $Vds = 0$ V to 50 V in 2-V steps. Measured (∘), modeled (solid lines), and quiescent point (dot).

from the gate for the first three harmonics also shows good agreement with the measured data, as shown in Figs. 15 and 16. The input reflected power measurements can be used to

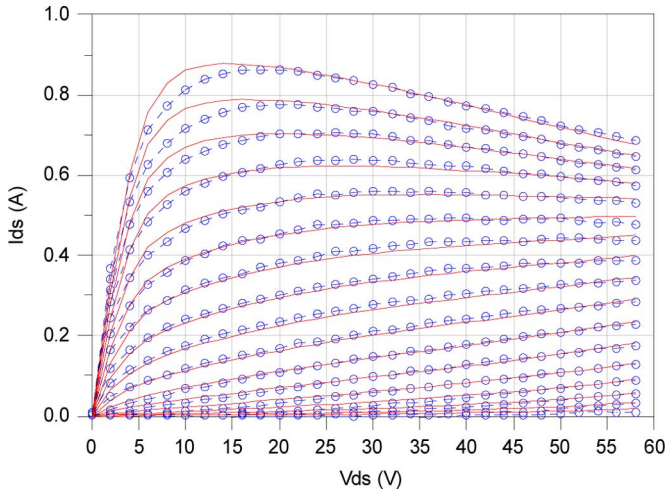

Fig. 13. Static *IV* characteristics for $Vgs = -11.0$ V to -3.0 V in 0.5-V steps, $Vds = 0$ V to 58 V in 2-V steps. Measured (∘) and modeled (solid lines).

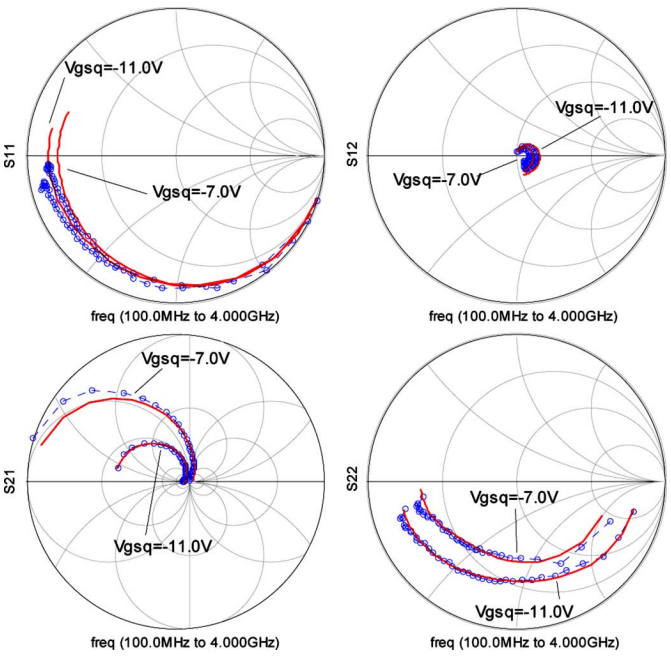

Fig. 14. S-parameters at $Vgs = -10$ V, $Vds = 55$ V and $Vgs = -7.0$ V, $Vds = 55$ V from $f = 0.1$ to 4.0 GHz. Measured (∘) and modeled (solid lines).

compute the actual power delivered into the device, which may be helpful in understanding and improving the efficiency of high power circuits.

Measuring and characterizing the harmonic power generation at both ports provides a better understanding of the device nonlinearities such as the terminal impedances and harmonic generation under large-signal excitation. The power measurements are of the unmatched device and not of a particular amplifier implementation, which further establishes this as a general device model.

Under large-signal continuous wave (CW) drive, the device will experience an increased static drain current due to large-signal nonlinearities and clipping. As a result, the static drain current rises with increasing incident RF power. This

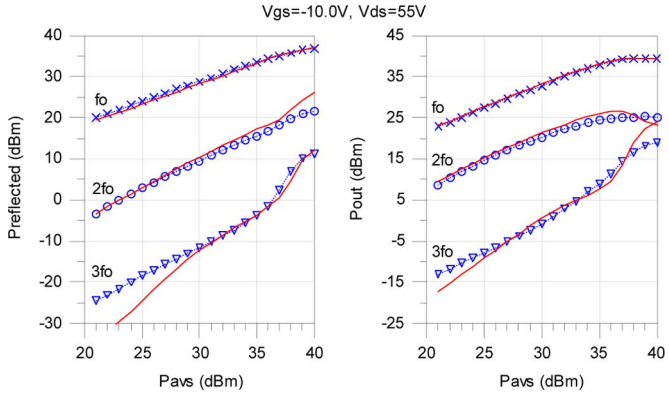

Fig. 15. Input reflected and output power versus $P\mathrm{avs}$ at $fo = 2$ GHz for three harmonics at $V\mathrm{gs} = -10$ V, $V\mathrm{ds} = 55$ V. Measured (symbols) and modeled (solid lines).

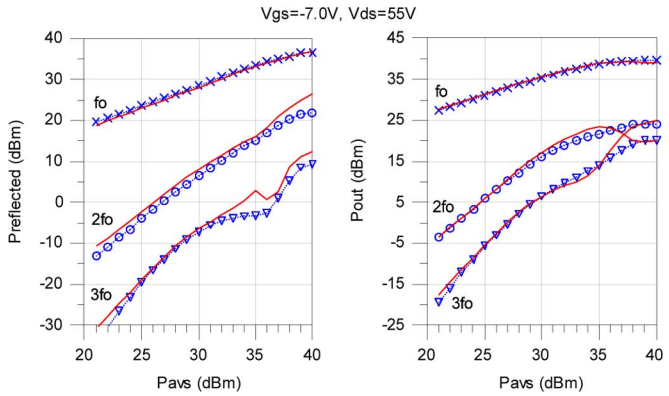

Fig. 16. Input reflected and output power versus $P\mathrm{avs}$ at $fo = 2$ GHz for three harmonics at $V\mathrm{gs} = -7$ V, $V\mathrm{ds} = 55$ V. Measured (symbols) and modeled (solid lines).

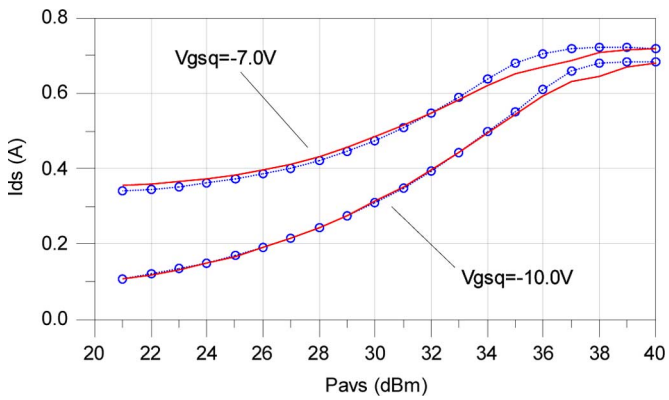

Fig. 17. Static drain current versus $P\mathrm{avs}$ at $fo = 2$ GHz for two biases of $V\mathrm{gsq} = -10$ V, $V\mathrm{ds} = 55$ V and $V\mathrm{gsq} = 7$ V, $V\mathrm{ds} = 55$ V. Measured (symbols) and modeled (solid lines).

effect leads to changes in the static dissipated power, and thus, creates variations in device temperature. A well-developed thermal model is necessary to predict this change in static drain current. The modeled and measured static drain current versus incident power from 21 to 40 dBm is shown in Fig. 17 for the biases of $V\mathrm{gs} = -10$ V, $V\mathrm{ds} = 55$ V and $V\mathrm{gs} = -7$ V, $V\mathrm{ds} = 55$ V. The model shows good agreement with the measured data signifying that it is capable of predicting the changes in static $I\mathrm{ds}$ with increasing RF drive power and the saturation of static $I\mathrm{ds}$ at high power levels.

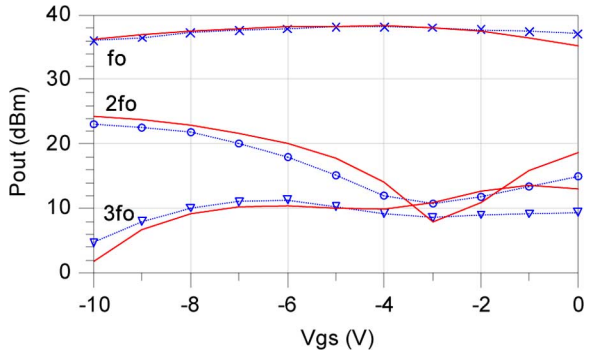

Fig. 18. Output power versus $V\mathrm{gs}$ for $V\mathrm{ds} = 55$ V with an incident power of $P\mathrm{avs} = 33$ dBm. Measured (symbols) and modeled (solid lines).

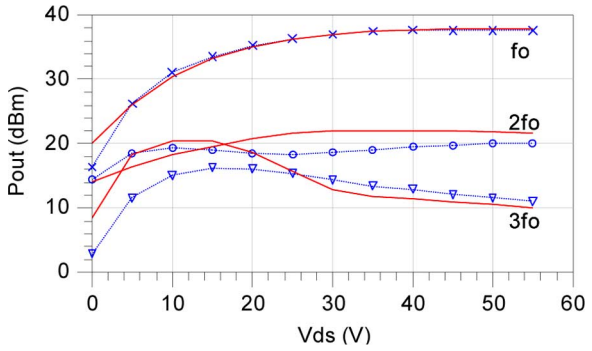

Fig. 19. Output power versus $V\mathrm{ds}$ for $V\mathrm{gs} = -7$ V with an incident power of $P\mathrm{avs} = 33$ dBm. Measured (symbols) and modeled (solid lines).

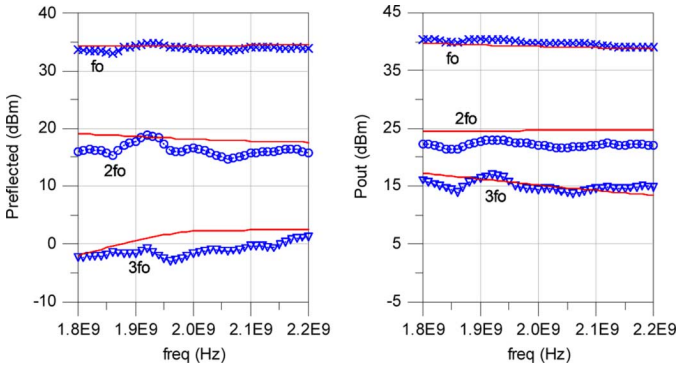

Fig. 20. Input reflected and output power versus frequency with an incident power of $P\mathrm{avs} = 37$ dBm over a 20% fractional bandwidth centered at $fo = 2$ GHz for three harmonics at $V\mathrm{gs} = -8$ V, $V\mathrm{ds} = 55$ V. Measured (symbols) and modeled (solid lines).

Additional characterization of the large-signal behavior of the device versus bias was performed in which the output power is measured across gate–source and drain–source voltages. The output power curves are shown as a function of $V\mathrm{gs}$ and $V\mathrm{ds}$ in Figs. 18 and 19, respectively. The model shows good agreement with the measured data for three harmonics.

D. Large-Signal Power Versus Frequency

The large-signal performance of the model versus frequency has been assessed over a moderate band of frequencies. Fig. 20 shows modeled and measured data over a frequency range which covers the GSM 1800, GSM 1900, CDMA 1900, WCDMA 1900, and WCDMA 2100 commercial communications bands. This represents a range of 20% fractional

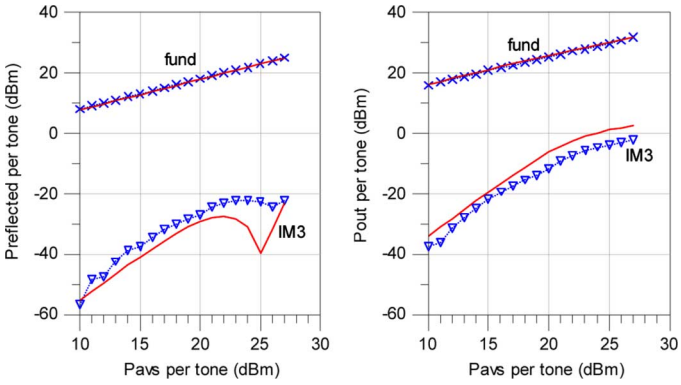

Fig. 21. Input reflected and output fundamental and third-order intermodulation products with $f1 = 2$ GHz and $f2 = 2.000\,1$ GHz at $V\mathrm{gs} = -8$ V, $V\mathrm{ds} = 55$ V. Measured (symbols) and modeled (solid lines).

bandwidth centered around 2 GHz with the device biased at $V\mathrm{gs} = -8$ V and $V\mathrm{ds} = 55$ V. A perusal of the data and model computations demonstrates the efficacy of the model in predicting output and input reflected power for three harmonics over this frequency range.

E. Third-Order Intermodulation Distortion

The third-order intermodulation distortion of the device has been characterized using a two-tone test, which was conducted on the device with $f1 = 2$ GHz and $f2 = 2.0001$ GHz over an incident power range of 10 to 27 dBm per tone with the device biased at $V\mathrm{gs} = -8.0$ V, $V\mathrm{ds} = 55$ V. Since the device is unmatched, significant third-order intermodulation products will be generated at both the output and input reflected ports. The measurement and modeled third-order intermodulation power is shown in Fig. 21. According to the data and simulated output, the model is capable of accurately predicting both output and input reflected third-order intermodulation products.

IV. Conclusion

A large-signal model for SiC MESFETs with a self-heating thermal model has been presented. A generalized current equation based on the Chalmers model, a thermal relationship, and a trapping correctional model has been presented. The drain-current model has demonstrated the ability to model pulsed-gate *IV* characteristics and pulsed-gate-and-drain *IV* characteristics under various quiescent biases, as well as static *IV* characteristics. The large-signal model has been implemented in Agilent Technologies' ADS and can accurately predict the small-signal S-parameters and the large-signal output and input reflected power of the device for three harmonics across bias and frequency. The large-signal model has also demonstrated the model's capability in predicting third-order intermodulation distortion.

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